MAN1944

SYSTEM OPTION CONTROLLER
User Guide

Revision Ø
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PRIME
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Performance characteristics are
subject to change without notice.

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ILLUSTRATIONS

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FOREWORD

This user guide contains detailed installation and programming information for the Type 3006 through 3025 System Option Controllers (SOC).

The SOC provides a four-channel serial interface and one or two buffered parallel I/O channels, which the user can employ in any combination to interface custom devices or communication lines. It also includes line frequency and programmable real time clocks plus an optional watchdog timer.

This user guide provides the user with all the information he needs to determine interface requirements, plan interconnections, and develop new software for custom devices. It describes all SOC features, including interface logic levels and timing, and defines the entire instruction set.

The SOC is also the basic interface for several standard Prime devices: Teleprinter and CRT Terminals, Serial Line Printer, Serial Card Reader, Paper Tape Reader and Paper Tape Punch. Separate user guides are provided with these devices to cover installation and specific programming, with particular emphasis on Prime drivers and standard software. However, users writing custom drivers for standard devices may want to refer to the detailed programming information in this user guide.

SECTION 1

INTRODUCTION

SCOPE OF HANDBOOK

This handbook provides information required to interconnect and program the Prime Type 3006 through 3025 System Option Controllers for use with custom I/O devices and communications or control interfaces.

The following Prime documents should be available for reference:

Document and Contents	Document No.
Prime System Reference Manual (Instruction set, addressing modes, input/output programming)	MAN1671
Prime Macro Assembler Language Reference Manual (Assembly language syntax and pseudo-operations)	MAN1673
Prime Installation and Maintenance (CPU physical characteristics, maintenance practices)	MAN1677
RTOS Reference Guide (Use of RTOS Executive and description of queue-driven real-time device drivers)	MAN1856
Wire List, Type 3006 to 3025 System Option Controller	WRL1529
Logic Diagrams for Types 3006 to 3025 System Option Controller	LDS1627
Program Listing BPIOT1 (Buffered Parallel I/O on S.O.C. Test No. 1)	LST0786.004
Program Listing RTCT2 (Real Time Clock Test)	LST0784.004
Program Listing TTYT2 (TTY Controller Test)	LST0783.006

The System Option Controller is the standard device interface for the Prime System Terminals, Paper Tape Reader/Punch and Character Printer. Users should review the following manuals for examples of existing applications and to avoid programming or hardware conflicts:

Document and Contents	Document No.
System Terminal User Guide (programming of CRT and TTY system terminals using serial asynchronous channels)	MAN1946
Paper Tape Reader/Punch User Guide (programming of paper tape devices through buffered parallel I/O channels)	MAN1947 (avail. 6/75)
Character Printer User Guide (programming of Character Printer using Serial asynchronous channel)	MAN1943 (avail. 7/75)

CAPABILITIES

The System Option Controller is a single etched circuit board that plugs into any available slot of the Prime CPU backplane. It is the basic controller for standard Prime peripherals such as the system terminal, paper tape reader/punch, character printer, and serially interfaced card reader. It may also be used to interface custom serial or parallel data devices or communication channels.

The board accomodates the following independent controllers (See Fig. 1-1).

Serial Interface, consisting of:

Asynchronous Line Controller. Provides independent asynchronous transmit and receive through any one of four independent ports.

Synchronous Line Control Capability. Enables ALC to communicate with synchronous lines at rates up to 50 KiloBaud.

One or Two Parallel Buffered I/O Channels

Each channel operates in half-duplex in full words or packed byte modes. Sixteen data lines, three input and three output control lines.

Clock Controller, consisting of:

Line Frequency Clock. Increments memory location at power line frequency and generates external interrupt when location overflows to 0.

Programmable Interval Clock. 16-bit counter that can be preset or read by the program. Countdown to zero causes a memory increment or external interrupt. The clock interval is 3.2 µs or 102.4 µs.

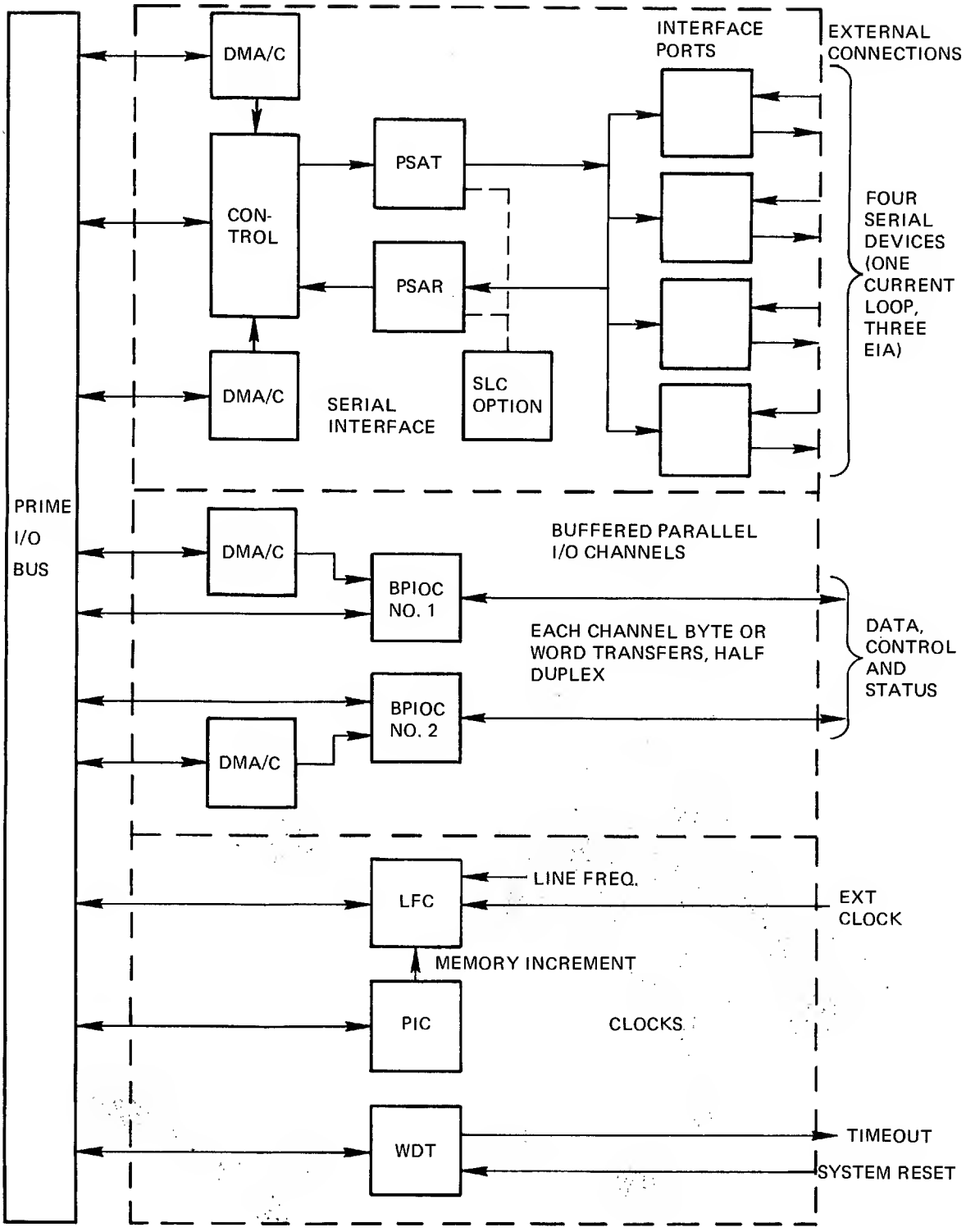


Figure 1-1. System Option Controller Block Diagram

Watchdog Timer. (Optional.) Generates an internal interrupt and optional master clear/auto restart if program fails to retrigger the WDT within 50 milliseconds.

Serial Interface

The Serial Interface provides flexible, low-cost interfacing between the Prime computer's parallel I/O bus and a large family of serially interfaced RS232C-compatible peripheral devices. With four independent, program-selectable input/output ports, a single controller is able to interface up to four serial full-duplex communication lines or local devices, one character at a time, in synchronous or asynchronous modes. Associated with each port is a pair of control signals - a control output and a status sense input - which can be used for ancillary control of EIA devices or as auxiliary serial data channels.

Asynchronous communication uses start and stop bits to synchronize each character transfer. Character length, data rate and transmit/receive connection (half /full duplex) are fully programmable.

Synchronous communication achieves message synchronization by transmitted sync characters and the identification of a match character while receiving. Bit timing is synchronized by an external modem clock.

Buffered Parallel I/O Channels

The SOC board provides one or two buffered input/output channels. They are identical except for device addresses. Each channel provides byte (8-bit) or word (16-bit) data transfers in a half-duplex input/output mode using a common 8- or 16-bit data bus. Each channel delivers data strobes to the associated external device and accepts status and ready inputs. Status and control signal levels are factory-defined and may be inverted on special order.

Clock Controller

This section of the board contains a line frequency clock (LFC), programmable interval clock (PIC) and an optional watchdog timer (WDT). These may be used singly or in combination for a variety of timing functions.

The LFC increments a memory cell at the power line frequency, at an external clock rate or on countdown of the PIC. When the incremented cell overflows to 0, an external interrupt is generated.

The PIC increments a 16-bit counter at a 3.2 µs or 102.4 µs rate. When the counter overflows to 0, an external interrupt is generated or the LFC memory cell is incremented.

The WDT is program-triggered into a 50 ms timeout cycle; if it is not re-triggered before timeout, the WDT provides an external timeout signal at the device interface and optionally initiates a system reset/auto restart or an internal interrupt through location '60 or both, under program control.

I/O Transfer Modes

The four controllers share the standard I/O interface but can be operated independently. They are all operable in PIO mode for the transfer of control and status information and for the transfer of data.

PIO mode includes interrupt control (vectored or standard) with programmable interrupt vectors. Interrupt control is such that any interrupt that occurs will hold off all other interrupts from the SOC until the interrupt has been acknowledged.

The Serial Interface and Parallel I/O Channels may optionally transfer data via DMA/C. The DMA/C control section samples each controller to determine whether there is a pending request. Upon detecting a request, the control section activates the standard DMA/C I/O control section on behalf of the requesting controller. At the end of the transfer, the control continues its scan. The sample rate is 5 MHZ. This means that the SOC can never use the I/O bus for two consecutive DMA/C cycles.

There are four separate programmable DMA/C channel address registers; one is for the receive section of the ASLC/SSLC, one for the transmit section, and one for each BPIOC.

The DMA/C may be enabled under program control for each option. Data transfers continue on each of the enabled sections (up to four simultaneously) until the CPU informs the channel that an end of range (EOR) has occured. The particular option that gets EOR ceases DMA/C data transfers and interrupts the CPU. Meanwhile, the remaining options continue their data transfers.

PERFORMANCE SPECIFICATIONS

Serial Transceiver

Data Ports

Number	4, operable one at a time
Types of I/O transfer	- Programmed I/O (INA, OTA) - Standard or vectored interrupt - DMA/C
Input/Output Levels	EIA RS-232C plus 20 mA current loop on asynchronous channel 1 only.

Asynchronous Communication

Data Format	Serial by bit, least significant bit first; characters demarked by start and stop bits plus optional parity bit.
Codes	5 to 8 data bits plus optional parity bit and 1, 1-1/2 or 2 stop bits
Data Rates	75 to 9,600 Baud
Teletype modes	4-wire full duplex or 2-wire echoplex.

Synchronous Communication

Data Format	Serial by bit, least significant bit first; character sync established by sync characters or external clock.
Codes	5 to 8 data bits plus optional parity bit.
External Clock Rates	DC to 640 KHz
Data Rates	75 to 19,200 Baud

Control Bits

Number	4 input/output pairs. Output is controlled by status register bit. Input is testable by SKS instructions.
Voltage Levels	EIA RS-232C compatible.

PERFORMANCE SPECIFICATIONS (Cont)

Parallel Buffered I/O Channels

Data Format	Parallel Byte (8-bit) or Word (16-bit). Input and output are half-duplex from common data bus.
Type of I/O Transfer	- Programmed I/O (INA, OTA) - Standard or Vectored Interrupt - DMA/C
Logic Levels	Standard or open-collector TTL (0, + 5V)
Control Outputs	- Two independent data strobes (handshake interface) - Device Enable (level)
Control Inputs	- Device data strobe (handshake interface) - Device Status and Ready (Levels tested by SKS instructions)

Line Frequency Clock (LFC)

Interval	Programmable: 1 to 65,536 periods of selected clock rate
Action on Timeout	Vectored interrupt
Clock Rates	
Line Frequency	50 or 60 Hz (local power line frequency)
External	User-generated
PIC Overflow	Programmable (see PIC)
External Clock Input	
Period	DC to 3 µs
Logic level	0, + 5V into TTL gate (See Section 3 for circuit)

PERFORMANCE SPECIFICATIONS (Cont)

Programmable Interval Clock (PIC)

Interval	Programmable: 1 to 65,536 periods of selected clock rate
Action on Timeout	Vectored External interrupt or LFC clock increment or both
Clock period	3.2 μs or 102.4 μs

Watchdog Timer

Interval between restart OCP's	50 ms max.
Action on Timeout	External timeout signal followed by optional internal interrupt through location '60 and system reset/auto restart.
External Timeout Output	Conducting NPN transistor output of opto-isolator switched out of conduction. (See Section 3.)
External System Clear Input	Positive voltage applied to photodiode of opto-isolator. (See Section 3).

SECTION 2

OPERATION

The System Option Controller has no external operating controls or indicators. Once it is configured and installed in the Prime CPU cabinet, it is controlled entirely by the program.

Before starting operation, make sure that any user-installed external equipment (peripheral devices, modems, etc.) is turned on and ready to operate.

User-installed external connections to the Watchdog Timer usually imply some operating procedures. For example, the timeout contact output may light an indicator, and the external reset connection may be used to restart the system after a WDT timeout. Operators should be informed of the required procedures.

SECTION 3

INSTALLATION AND CABLING

INSTALLATION AND BOARD CONFIGURATION

Mechanical Installation

The System Option Controller is a single, standard Prime plug-in circuit board that mounts in any vacant backplane slot. (In a 27-slot backplane, the SOC must be in one of the upper 17 slots.) External connections are made at the "top hat" edge connectors at the rear of the board Standard cables are available from Prime, or the user may fabricate custom cables using the Type 1421 connector kit.

Multiple SOC's Per System

More than one SOC may be used in a system, but each must have a different device address. Required jumper connections are shown in Sheet 47 of the drawing set, LDS1627. In addition, only one may control the I/O bus parity check functions. To disable parity, remove DIP 37C (wire wrap) or 49C (etch).

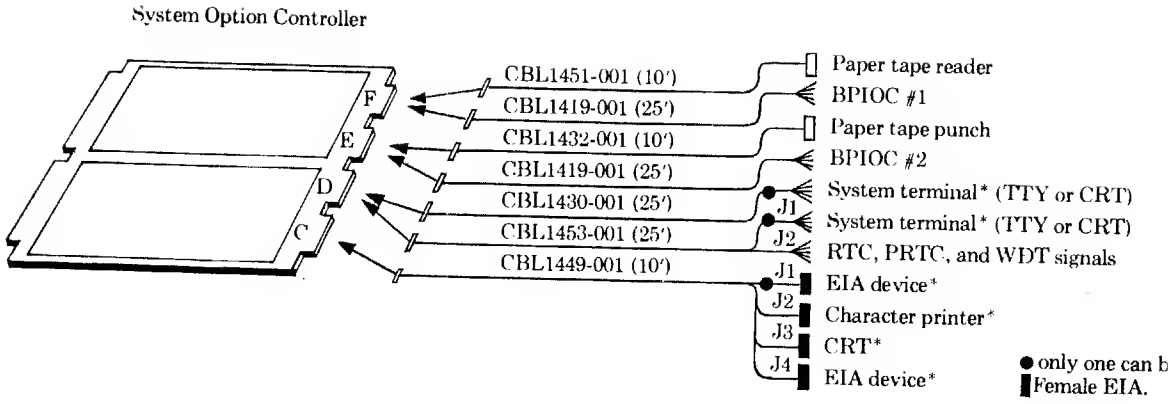
More than one LFC or PIC may be used simultaneously, since the LFC increment cell is program-selectable, and the clocks may be distinguished by different device addresses. However, it is not meaningful to have more than one watchdog timer.

CABLING AND INTERCONNECTIONS

Cable Selection

All external connections are made at the edge-connectors at the rear of the SOC board. Standard cables are available from Prime; see Figure 3-1 for cable identification numbers. Wire and connector pin identification drawings for the standard cables are reproduced at the end of this section. Signal pin assignments on the edge-connectors are defined in Tables 3-1 through 3-4. The user may also fabricate custom cables for special applications, using the Prime Kit 1421 consisting of a rear edge connector and mounting hardware. If a synchronous communication channel is used, a cable must be fabricated for edge connector C based on a 1421 Kit. (The synchronous clock lines are not brought out to EIA connector J3 of cable CBL1449-001.)

The SOC may be used both for standard I/O devices (paper tape reader/punch, user terminal, character printer, etc.) and for special user devices. Cabling is supplied with standard devices; the user only needs to order or fabricate special cabling for the custom devices. (Refer to the applicable device user guide for details.)



*One input device and one output device can operate simultaneously.
The four input and four output lines can accept any combination
of synchronous and asynchronous devices, however all enabled lines operate in only one mode at a time
Async. mode operation is standard; sync. mode operation is program selectable with option 3022.
Cables are supplied with devices.
System software supports the system terminal, paper tape reader/punch and character printer.

Figure 3-1. External Connections to S.O.C.

Table 3-1. EIA Serial Device Connections (Connector C)

Signal Name	Connector Pin	Description
EIAC4+	1	EIA Control Output Port 4
GND	2	
EIAC3+	3	" " " " 3
GND	4	
EIAC3+	5	" " " " 3
GND	6	
EIAC2+	7	" " " " 2
GND	8	
EIAC1+	9	" " " " 1
GND	10	
TXEIA3-	11	EIA Transmit Output Port 3
GND	12	
TXEIA4-	13	" " " " 4
GND	14	
TXEIA1-	15	" " " " 1
GND	16	
TXEIA2-	17	" " " " 2
GND	18	
EIAC1+	19	EIA Control Output Port 1
GND	20	
INBIT3-	21	EIA Control Input Port 3
GND	22	
INBIT4-	23	" " " " 4
GND	24	
INBIT3-	25	" " " " 3
GND	26	
INBIT2-	27	" " " " 2
GND	28	
INBIT1-	29	" " " " 1
GND	30	
INBIT1-	31	" " " " 1
GND	32	
RXEIA1+	33	EIA Receive Input Port 1
GND	34	
RXEIA2+	35	" " " " 2
GND	36	
PREXCL+	37	Synchronous Receive Clock Input (EIA)
GND	38	
RXEIA3+	39	EIA Receive Input Port 3
GND	40	
RXEIA4+	41	" " " " 4
GND	42	
PTEXCL+	43	Synchronous Transmit Clock Input (EIA)
GND	44	

Table 3-2. Current Loop Serial Device and Clock Connections (Connector D)

Signal Name	Connector Pin	Description
RXEIA1+	1	Connect together for current loop operation on
GND	2	Channel 1
CLIN+	3	
	4	
CLIN+	5	Current Loop input +
	6	
CLIN-	7	Current Loop input -
	8	
TXCL2-	9	Current loop transmit output, Channel 2
	10	
TXCL1-	11	" " " " " 1
	12	
TXCL3-	13	" " " " " 3
	14	
TXCL4-	15	" " " " " 4
	16	
	17	
	18	
TXCLR2+	19	Current loop transmit return, Channel 2
	20	
TXCLR1+	21	" " " " " 1
	22	
TXCLR3+	23	" " " " " 3
	24	
TXCLR4+	25	" " " " " 4
	26	
	27	
	28	
	29	
	30	
EXTCLK+	31	LFC External Clock Input, TTL levels
GND	32	
SCOPESY	33	
	34	For diagnostic use only. Do not connect
WDTTST	35	
	36	
WDTEXS-	37	
	38	WDT External Contact Output
RETOUT-	39	
	40	
EXPFI-	41	
	42	WDT External System Clear input
RETIN-	43	
	44	

Table 3-3. Buffered Parallel I/O Channel No. 2 External Connections (Connector E)

Signal Name	Connector Pin	Description
B20D01+	1	A Reg. Bit 9
GND	2	
B20D02+	3	" " " 10
GND	4	
B20D03+	5	" " " 11
GND	6	
B20D04+	7	" " " 12
GND	8	
B20D05+	9	" " " 13
GND	10	
B20D06+	11	" " " 14
GND	12	
B20D07+	13	" " " 15
GND	14	
B20D08+	15	" " " 16
GND	16	
B20D09+	17	A Reg. Bit 1
GND	18	
B20D10+	19	" " " 2
GND	20	
B20D11+	21	" " " 3
GND	22	
B20D12+	23	" " " 4
GND	24	
B20D13+	25	" " " 5
GND	26	
B20D14+	27	" " " 6
GND	28	
B20D15+	29	" " " 7
GND	30	
B20D16+	31	" " " 8
GND	32	
D2SKS-	33	Device Status Input
GND	34	
D2MVF-	35	Forward Data Strobe Output
GND	36	
D2RDY-	37	Device Ready Input
GND	38	
D20TA-	39	Device Enable Output
GND	40	
D2STRB-	41	Device Data Strobe Input
GND	42	
D2MVR-	43	Reverse Data Strobe Output
GND	44	

Word Mode: Right Byte
Byte Mode: Connect here. Left byte is transmitted first

Word Mode: Left Byte
Byte Mode: Not Used

Table 3-4. Buffered Parallel I/O Channel No. 1 External Connections (Connector F)

Signal Name	Connector Pin	Description
B10D01+	1	A Reg. Bit 9
GND	2	
B10D02+	3	" " " 10
GND	4	
B10D03+	5	" " " 11
GND	6	
B10D04+	7	" " " 12
GND	8	
B10D05+	9	" " " 13
GND	10	
B10D06+	11	" " " 14
GND	12	
B10D07+	13	" " " 15
GND	14	
B10D08+	15	" " " 16
GND	16	
B10D09+	17	A Reg. Bit 1
GND	18	
B10D10+	19	" " " 2
GND	20	
B10D11+	21	" " " 3
GND	22	
B10D12+	23	" " " 4
GND	24	
B10D13+	25	" " " 5
GND	26	
B10D14+	27	" " " 6
GND	28	
B10D15+	29	" " " 7
GND	30	
B10D16+	31	" " " 8
GND	32	
D1SKS-	33	Device Status input
GND	34	
D1MVF-	35	Forward Data Strobe Output
GND	36	
D1RDY-	37	Device Ready Input
GND	38	
D10TA-	39	Device Enable Output
GND	40	
D1STRB-	41	Device Data Strobe Input
GND	42	
D1MVR-	43	Reverse Data Strobe Output
GND	44	

Word Mode: Right Byte
Byte Mode: Connect here. Left byte is transmitted first.

Word Mode: Left Byte
Byte Mode: Not Used

Interface Circuits

Figures 3-2 through 3-4 show the SOC driving/receiving circuits and recommended matching circuits for all types of user connections.

Effects of Cabling on EIA Signal Distortion

With 100' of Belden type 8445/8456 cable, there will be no more than 2% distortion at 19.2 KBaud. With 10' of Belden type 8445/8456 cable, there will be no more than 2% distortion at 50KBaud. These values are computed as follows:

distortion = [(cable length (ft) X capacitance (pF/ft) + 330pF)
X 400 ohms (effective impedance) X 10^{-6}] X 100
/ [1 bit time (in μsec)]

e.g. Belden type 8445 (5 conductor) cable is 20 pF/ft

distortion = 100'X 20 X 400 X 10^{-6} X 100/50
= 80/50
= 1.6%

SOC drivers are EIA Type 1488 with 300 pF slew control. The receivers are EIA Type 1489.

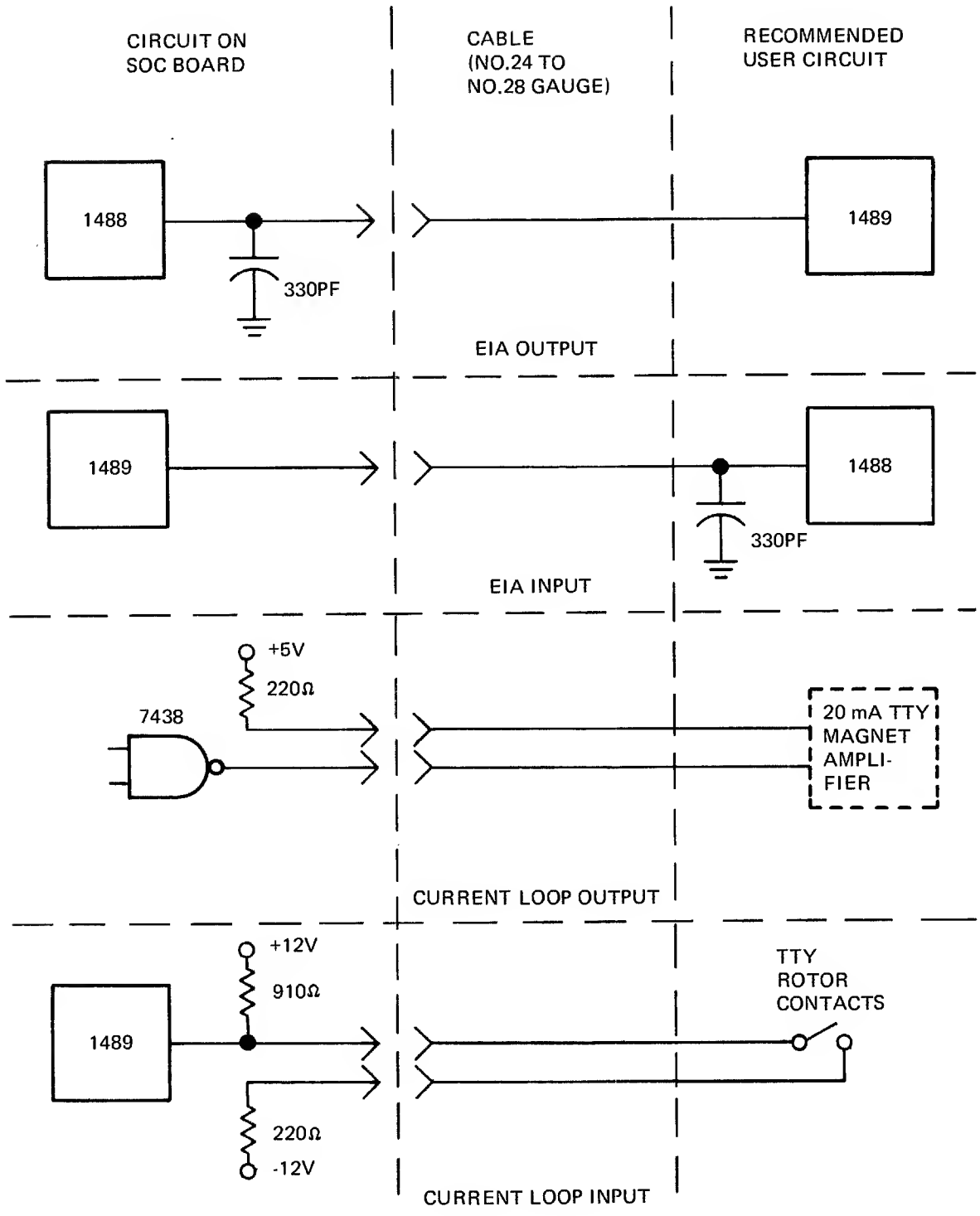
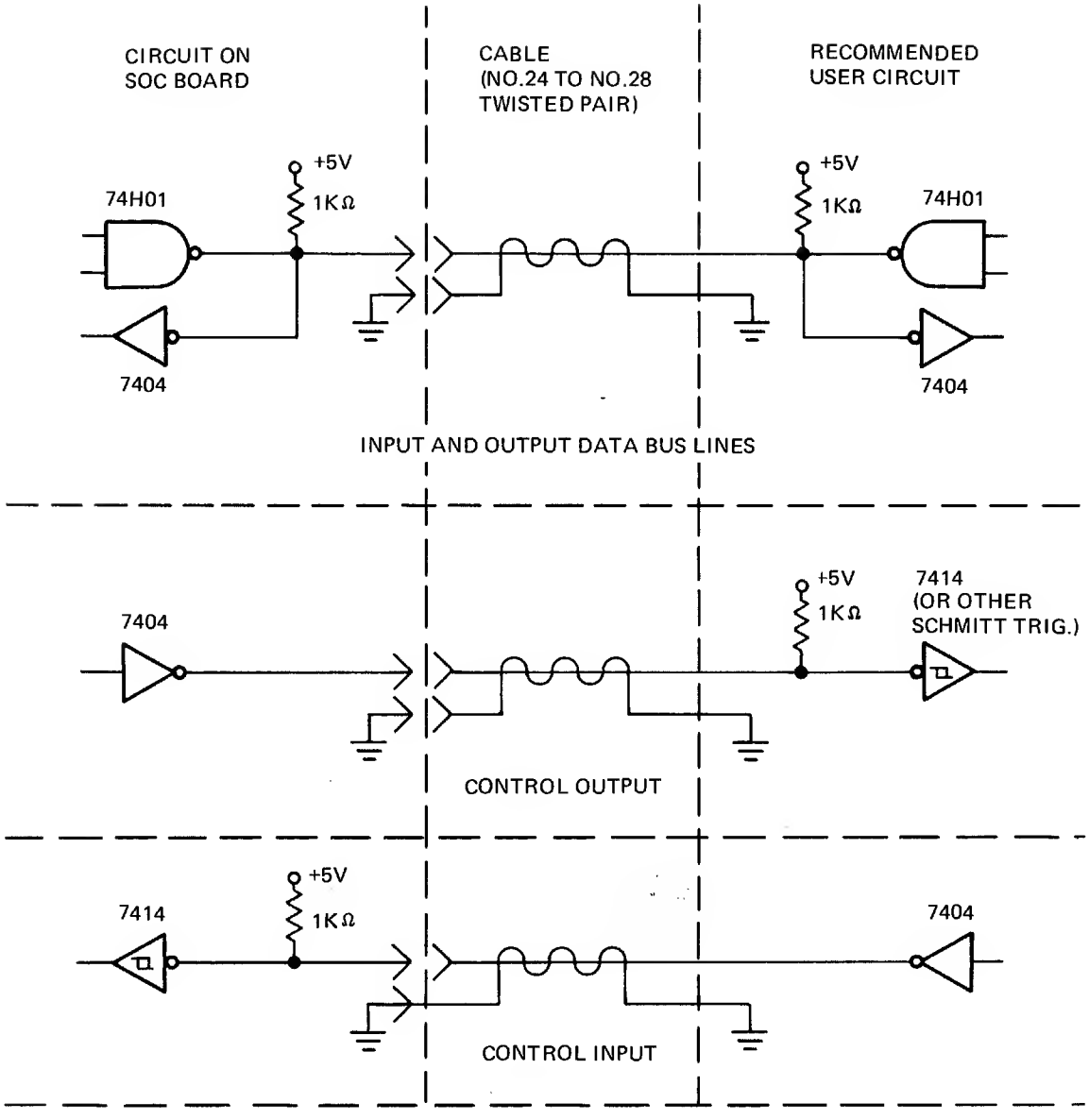


Figure 3-2. Serial Asynchronous/Synchronous Interface Logic Circuits



CABLE LENGTH (FT)	SETTLING TIME
10	200 ns
25	500 ns
100	2 μs

Figure 3-3. BPIOC Data and Control Interface Logic Circuits

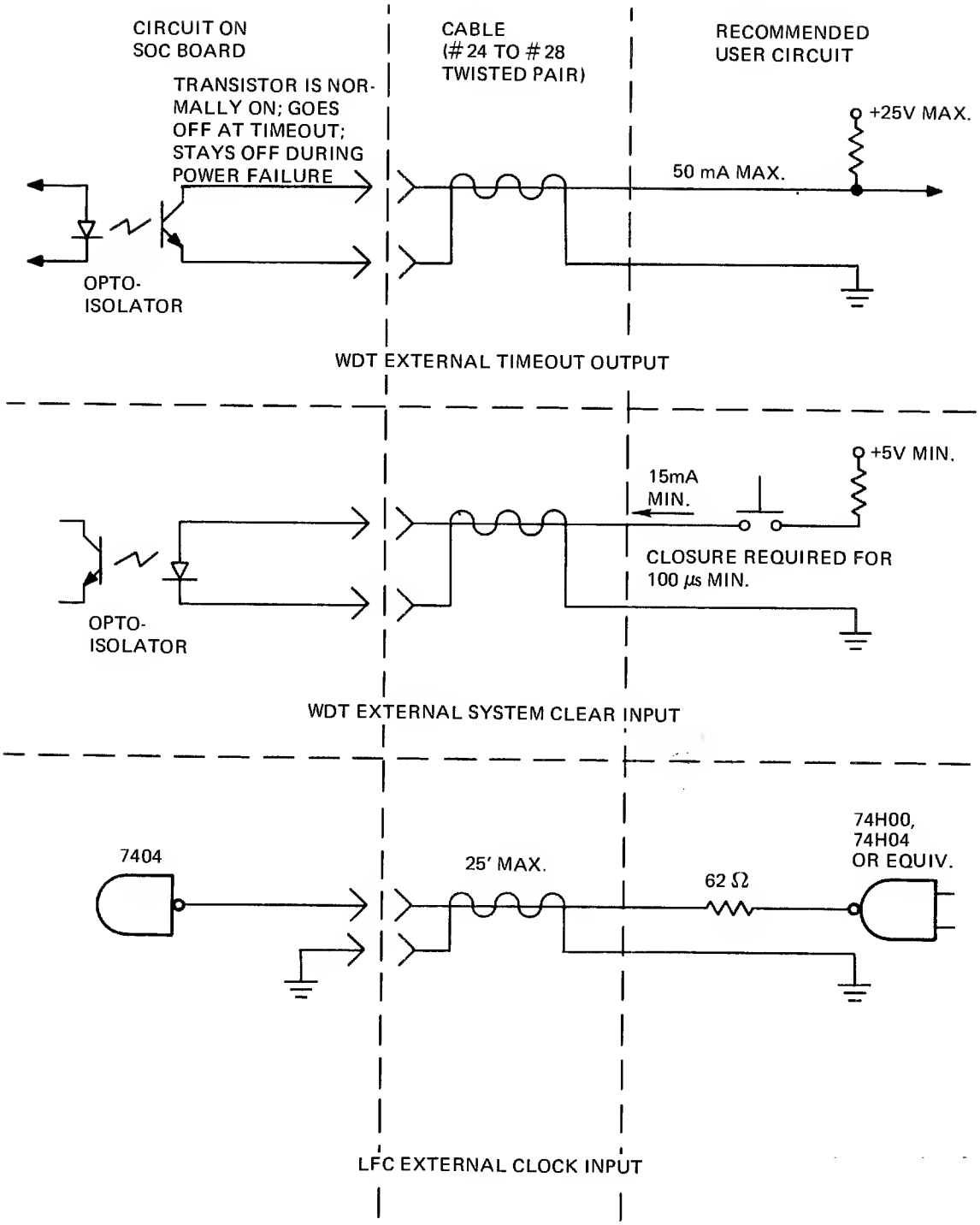


Figure 3-4. WDT, LFC External Connections, Interface Logic Circuits

SECTION 4

SYSTEM LEVEL PROGRAMMING

Prime FORTRAN, IOCS, DOS, DOS/VM and RTOS provide device drivers and function calls to support standard Prime devices connected to the serial interface and BPIOC. The following serial interface ports and BPIOC channels have permanent assignments:

Device	SOC Section	IOCS and FORTRAN Default Logical Device Assignments
System Terminal (ASR or CRT)	Serial Interface Port 1	01
Serial Card Reader	Serial Interface Port 4	09
Character Printer	Serial Interface Port 2	04
Paper Tape Reader	BPIOC No. 1	02
Paper Tape Punch	BPIOC No. 2	02

Serial interface Port 3 is reserved for a second CRT terminal or character printer.

The standard software assumes that the system terminal (either a Teletype or a CRT terminal) is connected to serial data Port 1 of the SOC and is operating at 110 Baud. The CRT may also be operated from Port 1 at higher operating speeds. This requires minor patches to the standard software (and bootstrap, in a disk system). See the Terminals User Guide for details.

For details on programming these devices, refer to the applicable user guides and the IOCS description in the Software Library User Guide. (See Section 1 for list).

In a system with a full complement of standard devices, custom options must be interfaced to a second SOC with a different device address. Appropriate device drivers can be generated according to the information in Section 5. However, it may be possible to modify a standard IOCS or RTOS driver and install it in the system.

The user may take advantage of an unused spare Serial Interface port or BPIOC channel to connect a compatible device. In this case, it may be possible to use the existing driver for that port/channel with little or no modification, and redefine its functions to apply to the custom device.

SECTION 5

ASSEMBLY LANGUAGE PROGRAMMING

This section contains a functional description and instruction set definition for each of the independent controllers on the SOC board. This information is required by users who intend to use the SOC board to interface custom I/O devices or communication channels and must write appropriate device drivers or control programs.

SERIAL INTERFACE

The Serial Interface controller provides four half/full duplex communication channels which operate in either asynchronous or synchronous mode. Associated with each channel is a pair of control bits (one input, one output) which can be used for ancillary control functions or as extra bit-by-bit communication line interfaces. Data transfers are controlled by Programmed I/O, Vectored Interrupts, or DMA/C transfers.

Asynchronous Line Controller (ALC)

The heart of the controller is an integrated-circuit Programmable Synchronous/Asynchronous Receiver (PSAR) and Transmitter (PSAT) that comprise two independent serial/parallel conversion channels.

The elements that are visible to the user are shown in Figure 5-1. Each section contains its own pair of control registers, interrupt vector and DMA/C channel registers, and control circuits for ready, busy, interrupt request and DMA/C request. All registers can be loaded or read by the program. In addition, there is a provision to input the controller's identification word (slot number and device ID).

Input and output data is processed by four interface ports which convert from internal logic levels to external current-loop or EIA voltage levels. One transmit port and one receive port can be enabled at a time. In addition, four input control bits can be tested by SKS instructions, and four control output bits are supplied to the outside world from the control registers.

The PSAR/PSAT can be operated in serial asynchronous mode in which characters are demarked by start and stop bits; no external clock signals are required. As an option, the controller can operate in synchronous mode in which synchronization is obtained from sync characters in the data stream. The character to be identified as sync while receiving is programmable, as is the fill character that is transmitted during idle periods.

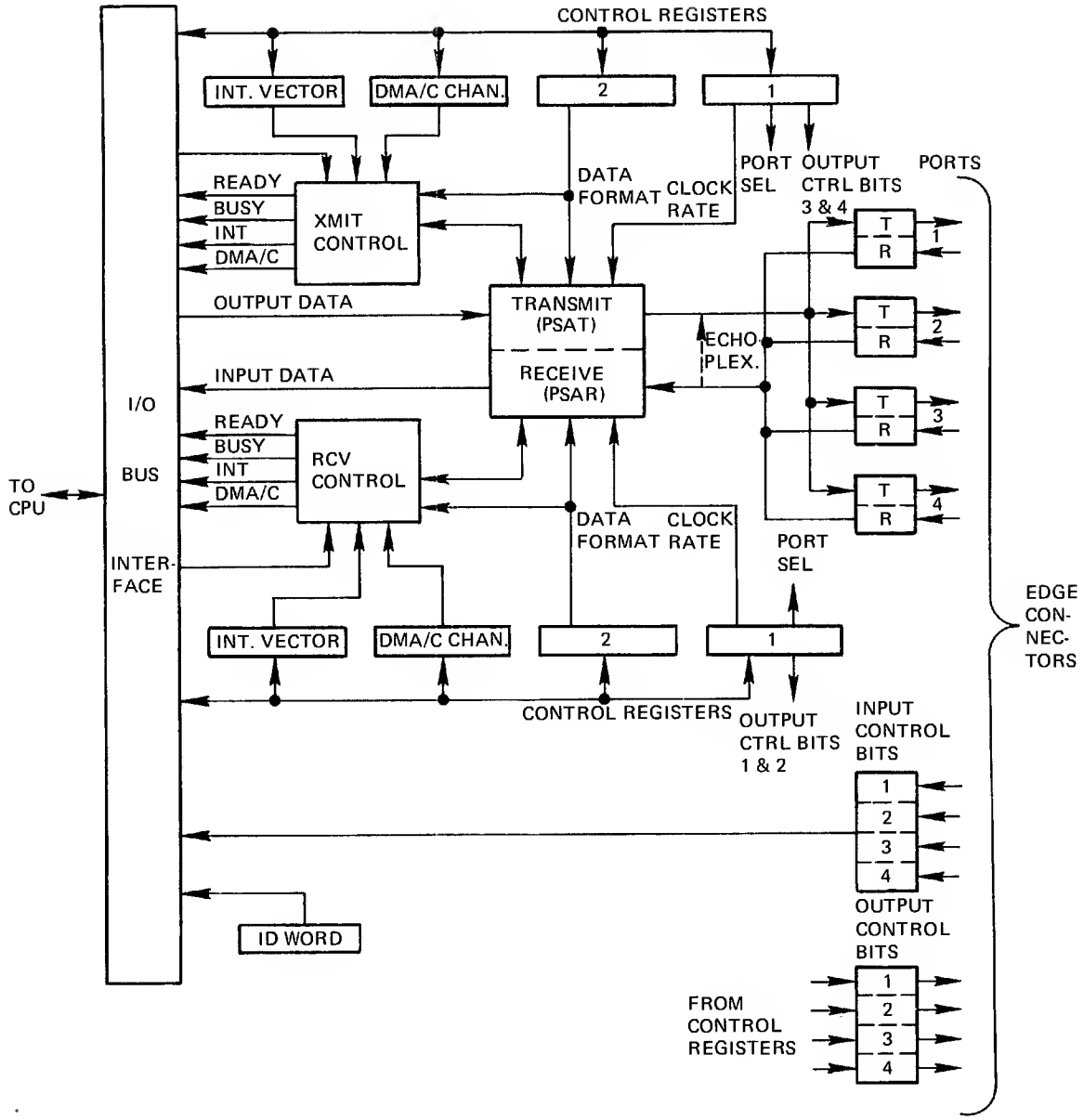


Figure 5-1. Serial Interface Block Diagram

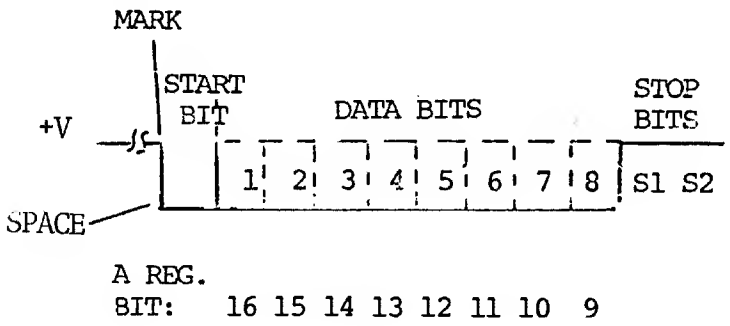
PSAT (Transmitter): To transmit a character serially, a parallel character is loaded into the PSAT's transmit buffer register by an OTA command. The PSAT adds START and STOP bits (and, optionally, a parity bit) and shifts the character out in the serial asynchronous mark-space format.

While the character is being shifted out, the processor may deliver another character to the the buffer register. Data transmission is continuous as long as a character is present in the buffer when the PSAT finishes shifting a character out. Whenever the buffer is empty, the transmit section presents a ready indication.

Serial output data can be connected to any one of the four output ports. All ports provide either 20 mA current loop or EIA level conversion. The output ports are accessible to the user on edge connectors at the rear of the controller board.

PSAR (Receiver): Serial inputs enter the controller at edge connectors and are converted to TTL logic levels. Input port No. 1 may operate either at 20 mA current mode or at EIA levels. The other ports accept EIA inputs only. The serial data entering one port is presented to the PSAR for assembly. The PSAR monitors the selected input for a START bit transition, and then samples the input line at the predetermined bit rate and assembles a character. When the character's stop bits are detected, the PSAR discards the START and STOP bits (and parity bit, if used), stores the character in a buffer register, and supplies a ready indication to the controller. Assembly of serial input bits continues, but the processor has a full character time to input the waiting character by an INA command, which clears the ready indication.

Serial Asynchronous Data Format: The format of a serial character at TTL levels is:



The EIA format is inverted, with a mark transmitted as -12 volts and received between -3V and -25V. A space is transmitted at +12 volts and received between +3 volts and +25 volts. An open line is received as a mark.

The current loop signals are marking when twenty millamperes of current flows in the loop, and spacing when no current flows.

Control Registers

Each section of the Serial Interface contains two control registers which control the operating characteristics of the PSAR/PSAT and select the data format, clock frequency, and transmit/receive ports. The registers may be loaded or read by the program and are initialized by a master clear. Each set of registers (one pair for transmit and another identical pair for receive) have the characteristics shown in Figure 5-2.

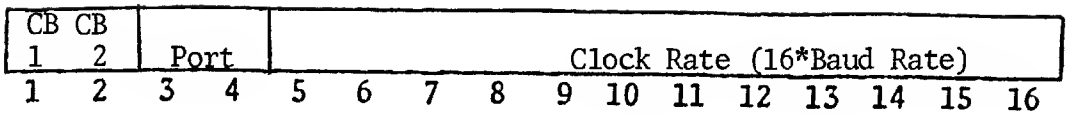
Control Output Bits: Control register 1 of each section provides two control output bits:

Register		Control Output Bit to Port:
RCV	CB1	1
	CB2	2
Xmit	CB1	3
	CB2	4

Control output bits 1 through 4 are run through an EIA-compatible interface to provide ancillary control to any EIA-compatible device. They may be programmed as extra "bit banger" serial data outputs. A one copied from the A register produces an EIA "MARK": a zero produces an EIA "SPACE".

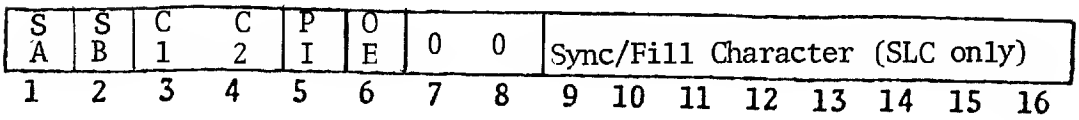
The control bits are independent of port selection. They appear at the interface whether or not the port is selected for serial data.

CONTROL WORD 1



CB1, CB2	Control Output Bits
Port	Port Select Code
Clock Rate	Determines internal PSAR/PSAT clock frequency

CONTROL WORD 2



SA	Synchronous/Asynchronous
SB	Number of Stop Bits
C1, C2	Character Length Code
PI	Parity Inhibit
OE	Parity Odd/Even

Figure 5-2. Serial Interface Control Word Formats

Port Select: Separate port select codes permit independent selection of one transmit port and one receive port. The codes are:

Control Word 1 Bit 03	04	Port
0	0	1
0	1	2
1	0	3
1	1	4

Clock Rate: Bits 5 through 16 of control word 1 determine the internal clock rate of the transmitter or receiver, as applicable. For asynchronous operation, the clock rate (CR) can be calculated in terms of the desired Baud rate by the following expression:

$$CR = 0.209715 \times (Baud)$$

The clock rate for synchronous operation is 1/16th the value above.

Following are octal values of N for commonly used clock rates:

Baud	N (Asynchronous)	N (Synchronous)
75	'17	
110	'27	
150	'37	
300	'76	
600	'175	
1200	'373	'17
2400	'767	'37
4800	'1756	'76
9600	'3735	'175

Synchronous/Asynchronous: Bit 1 of control word 2 is 0 for asynchronous operation. If the synchronous-mode option is present, a 1 selects synchronous communication.

Stop Bits: Bit 2 determines the number of stop bits for asynchronous operation. (For synchronous operation, this bit must be 0.)

SB	Stop Bits
0	1
1	2 (1-1/2 for 5 bit characters)

Character Length: Bits 3 and 4 determine the number of data bits per character (not counting stop or parity bits):

Bit: 03	04	Bits per character
0	0	5
1	0	6
0	1	7
1	1	8

Parity Inhibit: A 1 in bit 5 inhibits the character parity function; a 0 enables parity check and generation.

Parity Odd/Even: Bit 6 determines whether character parity is odd (0) or even (1).

Sync/Fill Character: This field of control word 2 is interpreted only in synchronous mode. For the PSAT, it defines a right-justified 5-to 8-bit character to be placed on the transmit output line as a fill character when no data is being transmitted. For the PSAR, it is the sync character to be identified during "search for sync" mode. (See later description of synchronous operation).

Modes of Operation

The mode of operation of the Serial Interface is assigned by OCP commands or control panel MASTER CLEAR:

Mode	OCP	Characteristics
Initialized Input	'0004 '1704*	Input only, echoplex, 110 Baud, 8-bit characters, no parity.
Initialized Output	'0104	Same as above but output only.
Prime Normal	'1204	Independent transmit and receive with echoplex. User must set up control registers.
Full Duplex	'1004	Independent full duplex transmit and receive. No keyboard echo. User must set up control registers.
Diagnostic	'1304	Self-test mode used by Prime Test and Verification software.

* Same as control panel MASTER CLEAR. Selects initialized input mode and also clears the interrupt masks and DMA/C enables.

Echoplex: In the echoplex modes, incoming characters are echoed to the originating terminal by a direct hardware connection to the output port. (See Figure 5-1.) The user must be careful not to transmit during an echo or the character will be garbled. This mode should only be used in four-wire connections.

Full Duplex: In the full duplex mode, the output and input channels are completely independent. This mode is intended for four-wire applications in which software supplies an echo to the originating terminal.

Diagnostic Mode: OCP '1304 disconnects all devices and connects the transmitter output to the receiver input, for wraparound self-testing. This mode is used mainly by Prime test and verification software.

Character Parity

The transmit and receive sections have independent parity check and generation capabilities. The parity function is enabled if the parity inhibit bit in control word 2 is a 0. The transmit section generates a parity bit and transmits it as an additional data bit. (Thus, 5-bit characters have 6 bits, and so on up to 9 bits maximum.) The receive section checks parity and, if there is an error, sets a flag which can be tested by SKS '1504. The parity bit is input to the A register along with the data bits, up to a maximum of 8 bits. Parity can be odd or even, depending on bit 6 of control word 2.

Framing Error

If there is no stop bit where one is expected, an internal flag is set which can be checked by SKS '1704.

Interrupts

There are two independent interrupt channels with separate enabling masks and programmable vector address registers. To enable an interrupt from a channel, the program must set one or both masks and, if vectored interrupt mode is enabled, provide the vector address(es). DMA/C must not be enabled. A ready condition in an enabled channel then causes an interrupt request. The ready signal that caused the interrupt is reset during the interrupt response. (If the other channel is also masked on and ready, it can then cause another interrupt request.)

Overrun Error

Double buffering permits a second character to be assembled while the preceding one is ready to be taken by the CPU. However, if the second character is assembled completely before the first is taken, the first character is lost. This condition sets an internal flag that can be tested by SKS '1604.

DMA/C

The transmitter and receiver can be enabled to initiate DMA/C cycle requests rather than interrupt requests during ready conditions. There are two independent enable flags and programmable channel address registers, one set for receive and one for transmit. To enable DMA/C requests, the program must load the appropriate channel address register(s) and enable the DMA/C flag(s). A ready condition in an enabled channel causes a DMA/C request. (No interrupt request results even if interrupt for the ready channel is masked on.)

When DMA/C end of range is detected, DMA/C is disabled and the ready condition for that channel is forced on. If the interrupt mask is set, this causes an external interrupt (standard or vectored, as selected by the program).

Programming Techniques

The procedure for operating the Serial Interface depends on the I/O technique - programmed I/O, Interrupt, or DMA/C.

For any mode, the user must set up the transmit and receive control registers for the desired mode of operation (half or full duplex), clock rate, port selection, and data format (number of bits per character, parity, number of stop bits).

For programmed I/O, the user tests the ready condition with the appropriate SKS, INA or OTA instruction to determine whether a character is ready to be received or transmitted.

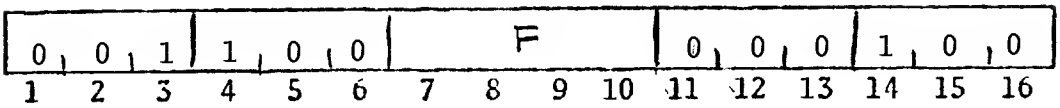
For interrupt-driven transfers, the user selects the interrupt mode (standard or vectored). The interrupt must be masked on by an OCP command, and in vectored mode, a vector address must be assigned to the transmit and receive sections by OTA commands. Thereafter, the user proceeds as in programmed I/O except that it is not necessary to test the ready condition by an SKS. When the interface is ready to transmit or receive another character, it issues an interrupt request which results in an effective JST to an interrupt handling routine. The routine must contain the appropriate INA or OTA instruction to handle the current data byte and, in the case of vectored interrupts, clear the active interrupt (CAI instruction).

For DMA/C controlled transfers, the program must set up address and range words in the appropriate memory locations, load the channel address register(s), and enable the channel. The interface then proceeds to request DMA/C cycles whenever the interface is ready for character transfer. The actual data transfers take place by memory cycle stealing, without program intervention. When a block transfer is

complete, an end-of-range interrupt occurs. This enables the program to set up another block transfer or terminate operation, as appropriate. Two DMA/C channels are available to the ALC so that the transmit and receive sections can operate independently, if desired. For details, see the DMA description in Section 5 or the DMC description in Section 6.

OCP Instructions

OCP 'F04 Output Control Pulse to Serial Interface



Perform the function specified by F in the Serial interface, as follows:

OCP '0004 Initialize for Echoplex Input

This mode is used for input from a Teletype or similar terminal. The transmit and receive control registers are initialized for 110 Baud, 8-bit characters, two stop bits, and parity disabled. Port 1 is selected for both input and output. Incoming data is echoed to the output port by the hardware; the result is equivalent to half-duplex operation of the terminal. A ready indication only occurs when an input character has been assembled; the transmitter always responds "not ready " to OTA '0004, so it is not possible to output a character. (Also see OCP '1704.)

OCP '0104 Initialize for Echoplex Output

This mode is used for output to a Teletype or similar terminal. The control registers are initialized as for OCP '0004, but only the transmitter can respond ready. Incoming data is assembled and echoed for half-duplex operation through port no. 1, but the receiver does not respond ready to SKS '0704 or INA '0004. The assembled character is stored, however, and if the interface is switched to input mode (OCP '0004) receive ready comes on immediately and the program can accept the waiting input character.

OCP '0204 Set Receive Interrupt Mask

Enables a receive ready condition to request an interrupt.

OCP '0304 Enable Receive DMA/C Operation

Enables a receive ready condition to request a DMA/C cycle. This flag is automatically reset when Receive End of Range is detected.

OCP '0404 Reset Receive Interrupt Mask and Receive DMA/C

OCP '0505 Set Transmit Interrupt Mask

Enables a transmit ready condition to request an interrupt.

OCP '0604 Enable Transmit DMA/C Operation

Enables a transmit ready condition to request a DMA/C cycle. This flag is automatically reset when Transmit End of Range is detected.

OCP '0704 Reset Transmit Interrupt Mask and Transmit DMA/C

OCP '1004 Enable Full Duplex Input/Output

Enables the transmit and receive sections of the Serial Interface to operate independently and cause ready indications. The control registers are not changed by this command; the user must specify bit rate, data format, input and output port, etc. Incoming data is not retransmitted; keyboard echoes must be generated by the software.

OCP '1104 Output Sync Pulse

Used in diagnostic mode to deliver an oscilloscope sync pulse.

OCP '1204 Enable Echoplex Input/Output

This is the normal mode used by most standard Prime system software. The transmit and receive sections of the Serial Interface operate independently and cause ready indications. The control registers are not changed by this command; the user must specify bit rate, data format, input and output port, etc. Incoming data is retransmitted as it is received for half-duplex operation through the selected output port. The user must be careful not to output a character for transmission while input is being received, or the echo will be garbled by the output.

OCP '1304 Set Diagnostic Mode

Disconnects all external devices and connects the output of the transmit section to the receive section for CPU-controlled diagnostic testing.

OCP '1504 Set Interrupt Masks

Sets both the receive and transmit interrupt masks.

OCP '1604 Reset Interrupt Masks

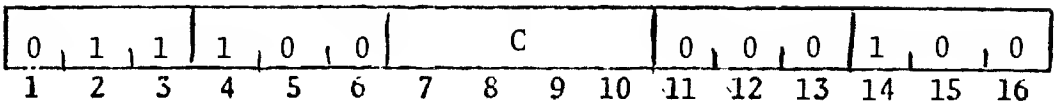
Resets both the receive and transmit interrupt masks.

OCP '1704 Initialize

Sets up the initialized input mode (see OCP '0004) and resets all Interrupt masks and DMA/C enables. Has the same effect as a control panel master clear.

SKS Instructions

SKS '0C04 Skip if Condition Satisfied



Skip the next instruction if the interface condition specified by C is satisfied as follows:

SKS '0004 Skip if Ready

Used in echoplex modes to test for either a transmit or receive ready condition (whichever is enabled). This instruction tests ready if:

Initialized input mode and receive ready

Initialized output mode and transmit ready

Input/output echoplex mode and either transmit or receive ready

SKS '0104 Skip if Not Busy

This instruction skips if:

Initialized input mode and no character being assembled

Initialized output mode and no character being disassembled

Input/output mode and neither receiver nor transmitter processing a character

The transmit section of the interface is busy from the time the first character is loaded by OTA '0004 into the transmit buffer until transmission of all characters is complete and the buffer is empty.

The receive section of the interface is busy from the time a device starts to transmit until slightly after "receive ready" is enabled.

Times required to transmit and receive characters depend on the clock rate and number of stop bits (both selected by control registers).

SKS '0204 Skip if Receiver not Interrupting

SKS '0304 Skip if Control Registers Valid

Skips if controller status is the same as the last control register setup OTA. (Notifies program if a master clear or OCP has changed the status since the last setup.)

SKS '0204 Skip if Receiver not Interrupting

SKS '0404 Skip if neither Receiver nor Transmitter Interrupting

SKS '0504 Skip if Transmitter not Interrupting

SKS '0604 Skip if Transmit Ready

Tests whether the transmitter (the PSAT) can accept a character from the A register (i.e., whether the transmit buffer is empty). Note that double buffering permits the interface to test busy and ready at the same time.

SKS '0704 Skip if Receive Ready

Tests whether the receiver is ready to transfer a character to the A register. (In initialized output mode, a character may be assembled but receive ready is disabled, so this instruction does not skip.

SKS '1104 Skip if Input Bit 1 is Marking

Note: Mark = EIA -12V or open line
Space = EIA +12V

SKS '1204 Skip if Input Bit 2 is Marking

SKS '1304 Skip if Input Bit 3 is Marking

SKS '1404 Skip if Input Bit 4 is Marking

SKS '1504 Skip if Parity Error

This happens if the received character has incorrect parity.

SKS '1604 Skip if Overrun Error

This happens if a second received character is completed prior to the first being taken by an INA.

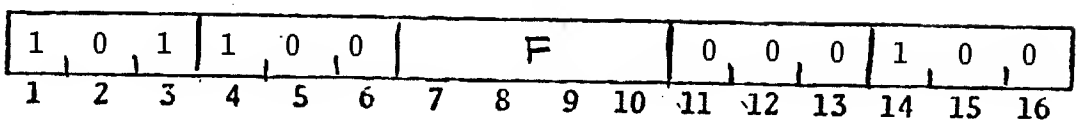
SKS '1704 Skip if Framing Error

This happens if there is no stop bit where one is expected.

The three error conditions (SKS '15, '16, '17) are accumulated on a message basis and are reset by OTA '0404.

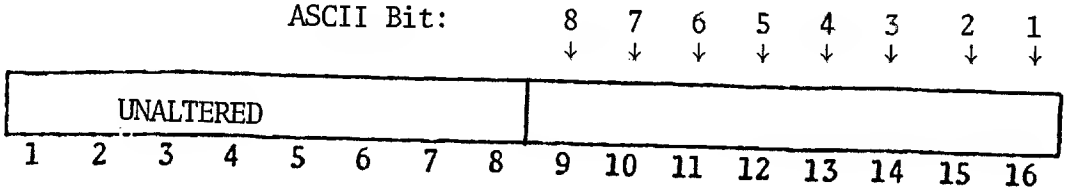
INA Instructions

INA 'F04 Input from Serial Interface



INA '0004 Input Character if Ready

If the receiver responds ready, this instruction logically ORs the assembled character into the right byte of the A register, clears receive ready, and skips the next instruction. (The left byte of A is unaltered.) If the receiver is not ready, or is in initialized output mode, this instruction acts as a NOP. ASCII code bits are transferred as follows:



Ready must be honored within one character time for continuous reception without loss of characters.

INA '0404 Input Receive Control Register No. 1

The transfer is unconditional; ready is not tested and the instruction always skips.

INA '0504 Input Receive Control Register No. 2

The transfer is unconditional; ready is not tested and the instruction always skips.

INA '0604 Input Transmit Control Register No. 1

The transfer is unconditional; ready is not tested and the instruction always skips.

INA '0704 Input Transmit Control Register No. 2

The transfer is unconditional; ready is not tested and the instruction always skips.

INA '1004 Clear A and Input Character if Ready

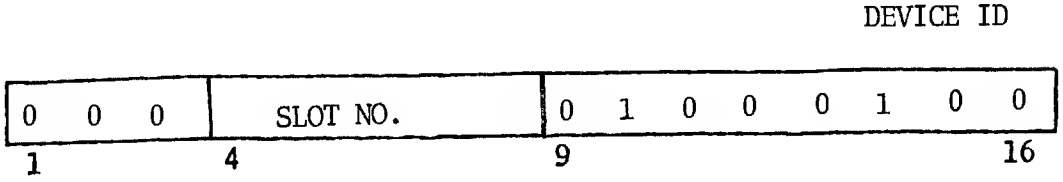
Same as INA '0004 but the A register is cleared before the character is loaded.

NOTE

For the following INA's, the transfer is unconditional and the processor always skips.

INA '1104 Input Device ID

Transfers the controller's identification number ('104) and backplane slot number to the A register:



INA '1404 Input Receive DMA/C channel address

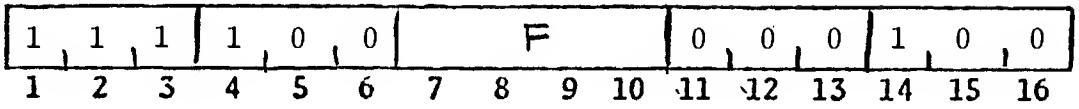
INA '1504 Input Transmit DMA/C channel address

INA '1604 Input Receive Interrupt Vector

INA '1704 Input Transmit Interrupt Vector

OTA Instructions

OTA 'F04 Output to Serial Interface



NOTE

OTA instructions '0004 through '0704 all test an internal busy indication that depends on completion of a previous OTA or an OCP 0, 1 or '17. Typical execution time is 25 μs. If busy, the instructions act as NOPs.

OTA '0004 Output Data Character if Ready

If the transmitter responds ready, this instruction transfers the right byte of the A register to the transmit buffer, clears ready, and skips the next instruction. If the transmitter is not ready, or is in initialized input mode, this instruction acts as a NOP.

OTA '0404 Output Receive Control Register 1

Also clears Parity, Framing, and Overrun error flags.

OTA '0504 Output Receive Control Register 2

OTA '0604 Output Transmit Control Register 1

OTA '0704 Output Transmit Control Register 2

NOTE

For all following OTA's, the transfer is unconditional and the CPU always skips.

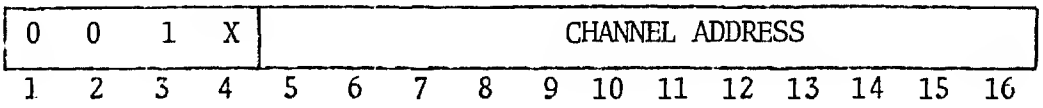
OTA '1404 Output Receive DMA/C Channel Address

The format is:

X = 0 for DMA, 1 for DMC

OTA '1504 Output Transmit DMA/C Channel Address

The format is:



X = 0 for DMA, 1 for DMC.

OTA '1604 Output Receive Interrupt Vector

Bits 1-4 must be 0.

OTA '1704 Output Transmit Interrupt Vector

Bits 1-4 must be 0.

Synchronous Line Controller (SLC) Option

The SLC option enables the Serial Interface to control synchronous serial communications lines operating to 50 KiloBaud. The information format is under program control and may be independently specified for receive mode and transmit mode. The operating speed depends on the external clock rate.

The SLC uses the PSAR/PSAT in the same way as the ALC already described, but start and stop bits are not used and the method of clocking differs. The SLC is operated with an externally provided modem clock. It is also provided with an internal clock for test purposes.

The receive section of the SLC is provided with a "Search for Sync" mode of operation. In this mode, the SLC searches for a match between an incoming bit stream and a programmed sync character. The SLC searches for two consecutive sync characters and then strips all succeeding sync characters. Once the message (one non-sync character) begins, the SLC leaves search-for-sync mode and provides ready indications for all succeeding characters.

The SLC transmitter places the sync character on the output line if the CPU does not provide a data character in time.

Both the receiver and transmitter may be operated in asynchronous or synchronous mode. Thus, the addition of the synchronous capability does not increase either the total number of lines that can be controlled (four receive and four transmit) nor the number of lines that can simultaneously be operated (one receive and one transmit).

Programming the SLC: The Serial Interface must be set up for mode of operation, data format and I/O mode (PIO, Interrupt, DMA/C) just as in asynchronous operation. The following additional operations are necessary:

1. Make sure bit 1 of control register 1 is a 1 and Bit 2 is 0.

2. Preset a sync match character code in Receive Control register 2 and preset a fill character in Transmit Control register 2.

3. Search for sync mode is entered by resetting the receiver (OCP '404), setting the interrupt mask and DMA/C if desired, and issuing the "Enter Search for Sync Mode" instruction (OCP '1404).

SLC Command Description: The standard device address of the SLC is '04. All instructions defined for asynchronous operation apply to the SLC, and the following instructions are added:

OCP '1404 Set Search for Sync Mode

SKS '1004 Skip if not in Search for Sync Mode

Programming Prime Asynchronous Peripherals

Standard Prime peripheral devices which connect through the Serial Interface are supported by Prime IOCS subroutines:

Device	IOCS Subroutine
Model 33/35 Teletype or CRT Terminal	I$AA01, O$AA01, C$A01 (low speed paper tape)
Character Printer	O$AL04
Card Reader	I$AC03

These subroutines enable users to communicate with the devices through standard FORTRAN formatted READ or WRITE statements or through symbolic assembly language calling sequences. For details, refer to the Prime Software Library User Guide.

For those users who need to communicate directly with a device, Table 5-1 summarizes the recommended instructions. Control word setups are specified in Table 5-2.

Card Reader Control Codes: The card reader supplies special status character codes and responds to certain control characters:

Octal	ASCII	Significance
	Output Control Characters	
'120	P	Pick card and start reading
'122	R	Reread last card
'021	X ON	Begin auto run
'023	X OFF	End auto run
	Input Status Characters	
'044	$	Reader ready to run
'012	.NL.	Start of record
'015	.CR.	End of record
'007	.BELL.	Hopper empty

Output characters are loaded into the A Register and delivered to the device by an OTA '0004. Status characters are input as normal data characters by INA '0004 or '0104. The program must test the character code.

Character Printer Ready: The character printer supplies a "device ready" indication on the EIA reverse channel. It appears on input control bit 2 or 3, depending on the active port, and can be checked by the appropriate input bit SKS instruction. If the printer is ready, the instruction skips.

Table 5-1. Instructions Used by Standard EIA Devices

Instruction	Application		
	ASR 33/35 or CRT Terminal	Character Printer	Card Reader
OCP '0204	Enable Keyboard Interrupt		Enable Card Character Interrupt
'0304			Enable Card DMA/C Requests
'0404	Disable Keyboard Interrupt		Disable Card Interrupt or DMA/C Requests
'0504	Enable Printer Interrupts	Enable Printer Interrupts	
'0604		Enable Printer DMA/C Requests	
'0704	Disable Printer Interrupts	Disable Printer Interrupts or DMA/C Requests	
'1504	Set Interrupt Masks		
'1604	Reset Interrupt Masks		
SKS '0004	Skip if Keyboard Ready	Skip if Printer Reader	Skip if Card Character Ready
'0104	Skip if Interface Not Busy		
'0404	Skip if Keyboard and Printer not Interrupting	Skip if Printer not Interrupting	Skip if Card Reader not Interrupting
'0504		Skip if Printer not Interrupting	
'1104			
'1204		Device on Port 2 Ready to Accept Data	

Table 5-1. (Cont)

Instruction	Application		
	ASR 33/35 or CRT Terminal	Character Printer	Card Reader
SKS '1304		Device on Port 3 Ready to Accept Data	
'1404			
'1704			
INA '0004	Input Keyboard Character if Ready		Input Card Character if Ready
'0404	Input Receive Control Register No. 1		
'0504	" " " " " 2		
'0604	Input Transmit Control Register No. 1		
'0704	" " " " " 2		
'1004	Clear A and Input Keyboard Character if Ready		Clear A and Input Card Character if Ready
'1104	Input Device ID		
OTA '0004	Output to Printer if Ready	Output to Printer if Ready	Output 'Pick Card' Code to Card Reader
'0404	Setup Receive Control Register No. 1		
'0504	" " " " " 2		
'0604	Setup Transmit Control Register No. 1		
'0704	" " " " " 2		
'1404			Setup DMA/C Channel Address
'1504	Setup DMA/C Channel Address for Printer Output		
'1604	Setup Keyboard Interrrupt Vector		Setup Card Interrupt Vector
'1704	Setup Printer Interrupt Vector	Setup Printer Interrupt Vector	

Table 5-2. Control Word Setup for Standard EIA Devices

Device	Control Word Settings	Notes
ASR Teletype	RC1 '000027 TC1 '000027	Port 1, 110 Baud
	RC2 '074000 TC2 '074000	ALC mode, 2 Stop bits, 8-bit Characters, parity disabled
Character Printer	RC1 '013735 TC1 '013735	Port 2, 9600 Baud
	RC2 '034000 TC2 '034000	ALC mode, 1 stop bit, 8-bit characters, parity disabled
CRT Terminal	RC1 '02RRRR TC1 '02TTTT	Port 3, RRRR = Receive clock rate, TTTT = Transmit clock rate
	RC2 '034000 TC2 '034000	ALC mode, 1 stop bit, 8-bit characters, parity disabled
Card Reader	RC1 '033735 TC1 '033735	Port 4, 9600 Baud
	RC2 '034000 TC2 '034000	ALC mode, 1 stop bit, 8-bit characters, parity disabled.

BUFFERED PARALLEL I/O CHANNELS (BPIOC'S)

Each SOC board contains one or two buffered parallel I/O channels. If they are not assigned to the Paper Tape Reader or Punch, they may be used as a parallel interface to user-installed equipment

Each BPIOC is a half-duplex channel that exchanges parallel data between the CPU and an external device in 8-bit bytes or 16-bit words. There is also a byte-packing mode in which a 16-bit word is input or output as two successive 8-bit bytes. During programmed I/O, data is exchanged between the CPU A Register and the external device. For DMA/C transfers, data goes directly to/from a CPU memory location. Single bytes are right-justified in the CPU word; in byte-packing mode, the left byte is transferred first.

Interface Signals

A block diagram of one BPIOC section is shown in Figure 5-3. In addition to the 16-bit bidirectional data bus, three control outputs are provided and three status/timing inputs are accepted from the device. All inputs and outputs operate at TTL levels and are assigned the following polarities at the factory:

Signal	Polarity
Device Ready	-T
Device Strobe	-T
Device Enable	-T
Forward Data Strobe	-T
Reverse Data Strobe	-T

The levels and the timing of the data strobes can be altered by jumper connections on the board. For details, see Appendix A.

The notation -T means the signal is negative (i.e., LOW, 0 volts) when asserted. To relate this to the signal name (mnemonic) conventions used in Prime logic diagrams and cable signal lists, note that the last character of a signal mnemonic specifies the output level of the signal when it is asserted (i.e., when the condition named by the mnemonic is true.) A plus sign (or no sign) means the signal is high (+2.4 to +5.0 Vdc) when asserted; A minus sign means the signal is low (0 to 0.4 Vdc) when asserted. For example, the DISTRB- (device strobe) signal is low when asserted.

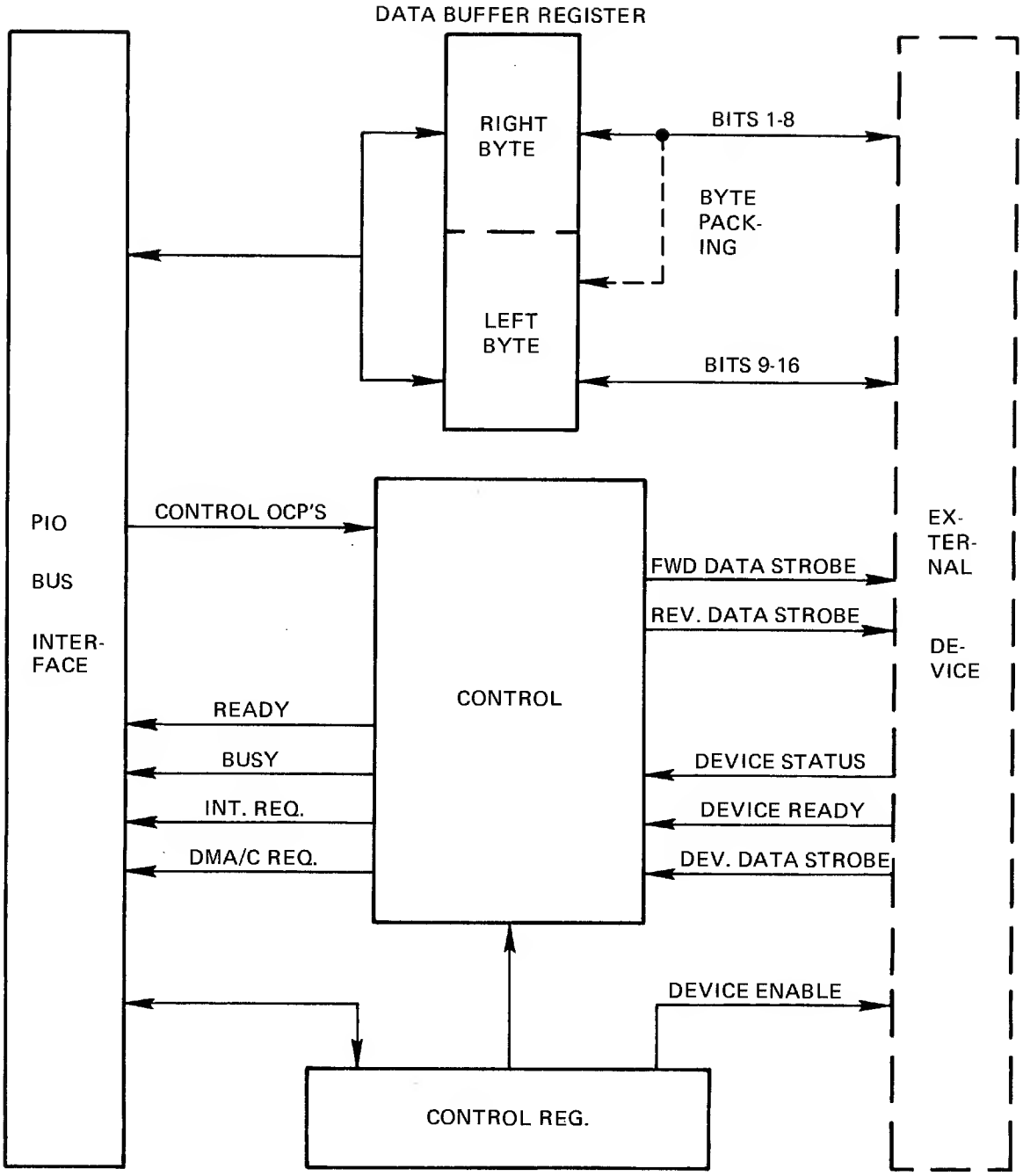


Figure 5-3. BPIOC Block Diagram

Device Synchronization (Handshake)

Data transfers between the BPIOC and the external device are synchronized by a handshake between Device Ready, Data Strobe, and Device Strobe signals. These signals are levels rather than arbitrarily timed pulses, so all transfers use the same asynchronous sequence regardless of device timing requirements. Figure 5-4 shows the input and output sequences in relation to PIO Ready and the right-byte-next flag.

Input Transfers (Figure 5-4A, B): In order for any transfer to take place, the Device Ready line must be asserted (i.e., the device must be turned on and ready to operate). The Data Strobe (forward, reverse or both) is then asserted in preparation for the transfer. When the device asserts its Device Strobe line, data is assumed to be stable on the data bus. The BPIOC drops the Data Strobe line to inform the device that the data is loaded in the buffer register, and also sets the PIO Ready internal flag. The device is expected to drop its device strobe in response to the trailing edge of the Data Strobe. The interface then waits for an INA instruction (or DMA cycle) to read the data to the CPU. When that occurs, PIO Ready is reset and the Data Strobe is asserted to request another data transfer.

For byte or word transfers (Figure 5-4A), the PIO Ready flag is cycled on and off for each transfer. In byte packing mode (Figure 5-4B), Ready stays off during the first byte and the Data Strobe is turned on by the trailing edge of Device Strobe.

Output Transfers (Figure 5-4C, D): In order for an output transfer to take place, the BPIOC must receive a data word by an OTA instruction and the Device Ready line must be asserted. When soon as the device raises the Device Strobe line, the Data Strobe is asserted to notify the device that data is waiting in the BPIOC buffer register. Once the device has accepted the data, it drops the Device Strobe, whereupon the BPIOC drops its data strobe and sets PIO Ready. When another word is received from an OTA instruction, the cycle repeats. In byte packing mode (Figure 5-4D), Ready stays off during the first byte and the Data Strobe is asserted in response to the next Device Strobe.

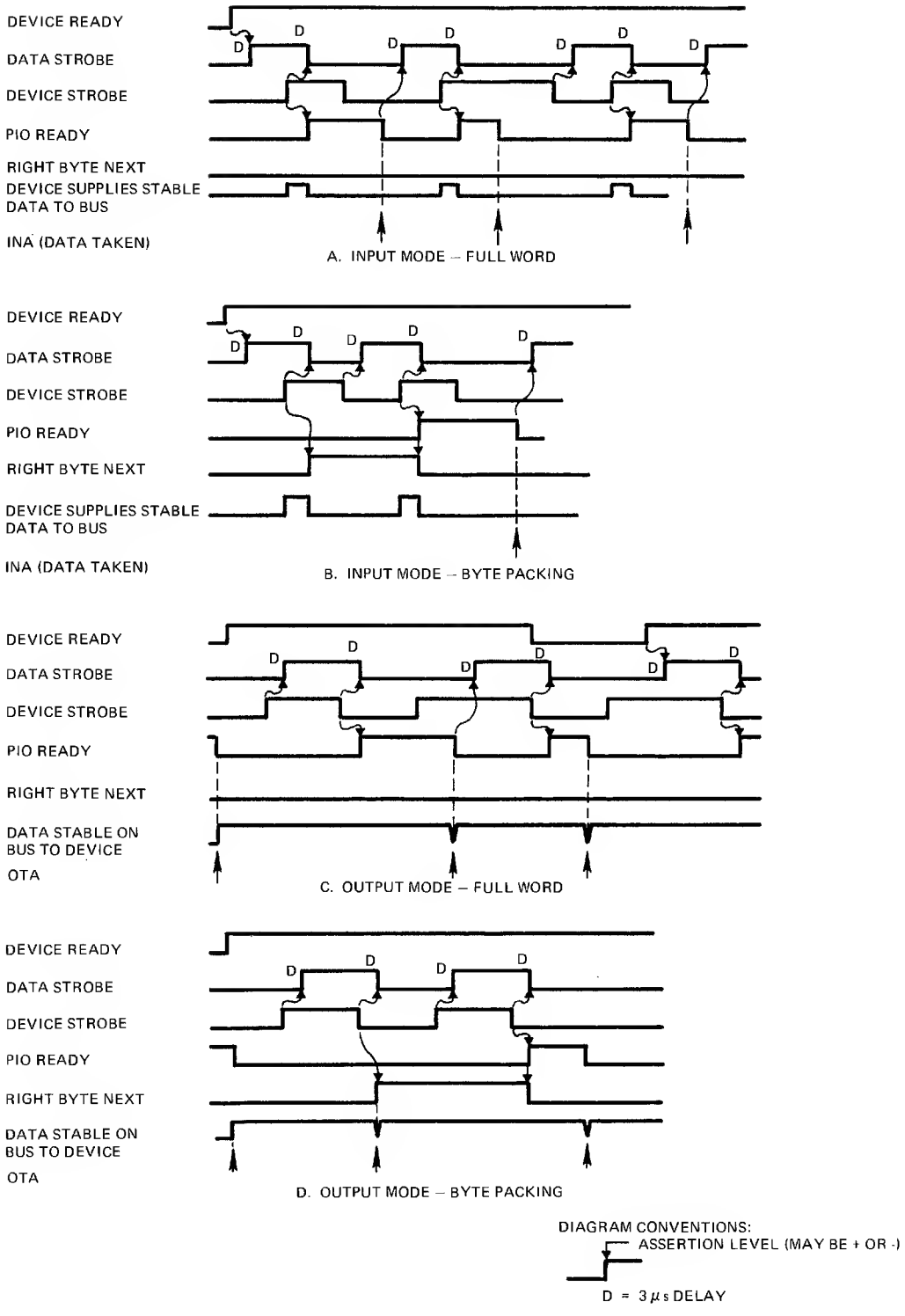


Figure 5-4. BPIOC Data Transfer Handshakes

Control Register

The BPIOC control register controls mode of operation (input/output), byte packing, strobe generation, and the device enable line as shown in Figure 5-5.

Mode of Operation: Each BPIOC channel is intended for half-duplex operation and can operate either in output mode or in input mode but both at a given time. The Input Mode is selected as the initialized condition and wired as such when the hardware is configured. Bit 13 of the control register switches the BPIOC to output mode.

Byte Packing: When byte packing is enabled by bit 14 of the control register, data is exchanged between the interface and the external device in 8-bit bytes. Transfers to and from the CPU consist of full 16-bit computer words. (See Figure 5-4.) During output, the two bytes in the A register are swapped into the BPIOC buffer (A bit 1 goes to to buffer bit 09).

Non-Byte Packing: When byte packing is disabled by a 0 in bit 14 of the control register, data is transferred between the device and the interface as a single 16-bit word.

Data Strobe Control: Bit 15 of the control register selects whether one or both of the data strobe lines to the device are asserted during data transfers. Table 5-3 shows which strobes are generated under various conditions.

The terms 'forward' and 'reverse' apply to a bidirectional device such as the paper tape reader. In a customer interface, they can be used for any desired function. For example, in an X-Y plotter interface, the forward strobe could deliver X-axis data and the reverse strobe could deliver Y-axis data.

Device Addresses

In the BPIOC instruction descriptions, a device address of XX is shown. XX has the following value for standard devices:

Paper Tape Reader	'01
Paper Tape Punch	'02
BPIOC No. 1	'30
BPIOC No. 2	'31

If more than two BPIOC channels are used, other device addresses must be assigned by modifying board jumper connections. (See Section 3.)

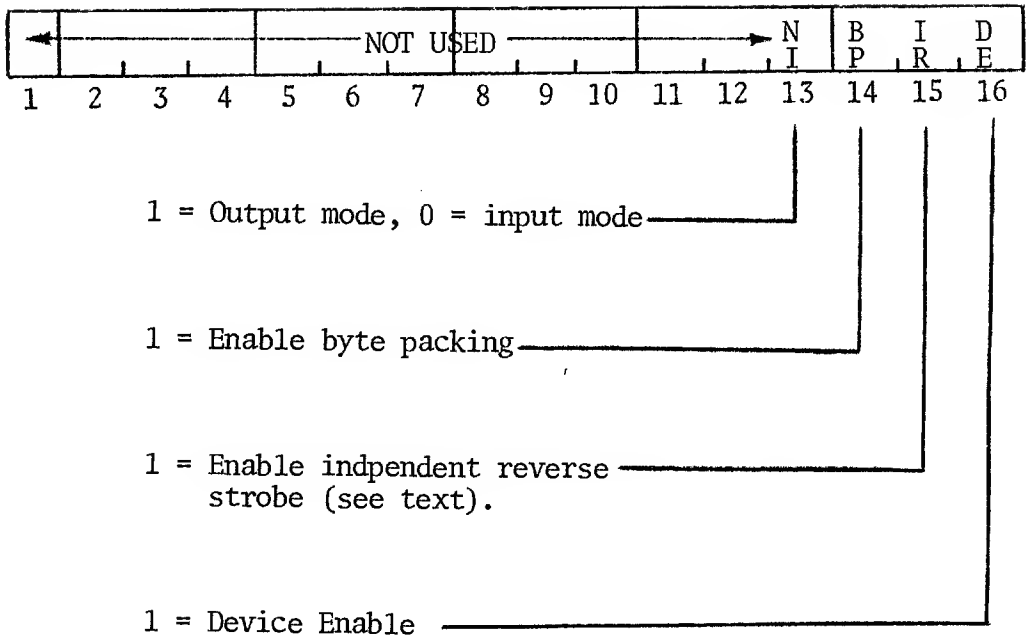


Figure 5-5. BPIOC Control Register Bit Assignments

Table 5-3. Conditions for Generating Forward and Reverse Strobes

Condition			Strobes Generated with Ind. Rev.	
FWD/REV	OFF/ON	INA or OTA	Wired But Not Enabled	Wired and Enabled (2)
FWD	OFF to ON Transition in Input Mode	-----	FWD	FWD REV
FWD	ON	Note 1	FWD	FWD REV
REV	OFF to ON Transition in Input Mode	-----	---	REV
REV	ON	Note 1	---	REV

NOTES

1. Strobes are generated under the following conditions:

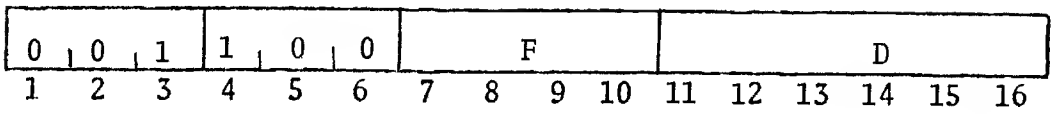
   a. INA '0030/31 or INA '1030/31 with the device ready line asserted and input mode in effect

   b. OTA '0030/31 with the device ready line asserted and output mode in effect

2. 'Enabled' means bit 15 of control register set

OCP Instructions

OCP 'FD Output Control Pulse to BPIOC Device D



Perform the function specified by F in the BPIOC device no. D (XX), as follows:

OCP '00XX Start

Enables the BPIOC to transfer data, resets the data register, and resets the right-byte-next flag.

OCP '01XX Stop

Prevents further data transfer. The BPIOC must be stopped prior to a change of direction or control register setup.

OCP '02XX Forward

Sets the forward/reverse flag.

OCP '03XX Reverse

Clears the forward/reverse flag.

OCP '14XX Enable DMA/C

Enables the BPIOC to issue a DMA/C cycle request instead of an interrupt request during a ready condition. Each channel has an independent DMA/C request line.

OCP '15XX Set Interrupt Mask

Enables the BPIOC to request an interrupt during a ready condition. The DMA/C flag must be cleared.

OCP '16XX Reset Interrupt Mask

Clears the interrupt mask.

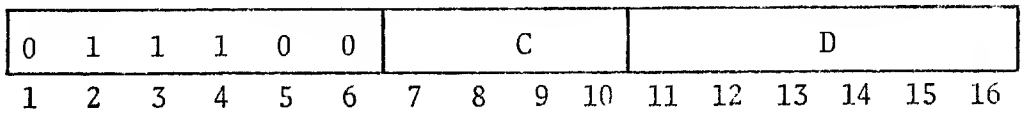
OCP '17XX Initialize

Sets the BPIOC to the following initial conditions:

Item	State
Start/Stop	Stop
Forward/Reverse	Forward
Data Register	Cleared
Right-Byte-Next	Reset (left byte next)
Interrupt Mask	Reset
DMA/C Enable	Reset
Control Register	Input mode. Non-byte-pack, disable independent reverse, and device not enabled

SKS Instructions

SKS 'DC Skip if BPIOC Device D Condition C Satisfied



SKS '00XX Skip if ready

Tests ready if:

Input mode and a word has been received (two bytes if in byte packing mode).

Output mode and the device has been given a word (two bytes if in byte packing mode).

DMA/C End of Range has been received.

SKS '01XX Skip if device ready line true

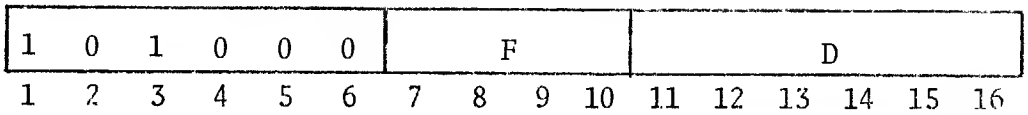
SKS '02XX Skip if right-byte-next flag is set

SKS '04XX Skip if BPIOC not interrupting

The BPIOC interrupts if it is ready in PIO (non-DMA/C) mode and has its mask set.

INA Instructions

INA 'FD Input Data Type F from Device D



INA '00XX OR Input Data Register to A if Ready

If the interface is in input mode and responds ready, this instruction logically ORs the character to the A register, resets ready, and skips the next instruction. If the channel is not ready or is in output mode, this instruction acts as a NOP.

INA '10XX Clear A and Input Data Register if Ready

Same as INA '00 but A is cleared prior to the operation if ready.

INA '11XX Input Device ID

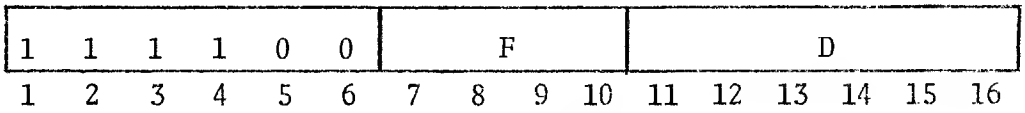
The ID of BPIOC (1) is '101. The ID of BPIOC (2) is '102.

INA '14XX Input DMA/C channel address

INA '16XX Input Interrupt Vector

OTA Instructions

OTA 'FD Output Type F to Device D



OTA '00XX Output A to Data Register if Ready

If the specified channel is in output mode and responds ready, this instruction transfers the A register to the channel data register, clears ready, and skips the next instruction. If the channel is not ready or is in input mode, this instruction acts as a NOP.

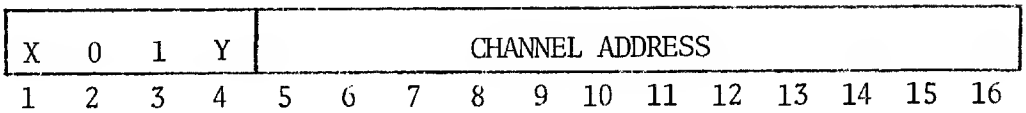
OTA '10XX Output Control Register

NOTE

For this and all subsequent OTA's, the transfer is unconditional and the next instruction is skipped.

OTA '14XX Output DMA/C Channel Address

The format is as follows:



X = 1 if input transfers, 0 if output

Y = 1 if DMC, 0 if DMA

OTA '16XX Output Interrupt Vector

Bits 1-4 must be 0.

CLOCKS (LFC, PIC and WDT)

The SOC provides two standard clock timing sections - the Line Frequency Clock (LFC) and Programmable Interval Clock (PIC). As an option, a Watchdog Timer (WDT) can be ordered.

The LFC increments a memory cell at one of three clock rates - the power line frequency, an external clock rate (user-provided) or on timeout of the PIC. When the incremented cell overflows from -1 to 0, an external interrupt is generated.

The PIC increments a 16-bit register that can be preset to a starting value under program control. The increment rate is either 3.2 µs or 102.4 µs, program selected. When the counter overflows to 0, an external interrupt is generated or the LFC memory cell is incremented and the register is automatically reset to the programmed value.

The WDT can be triggered by the program to enter a 50 ms timeout period. If another timeout is not initiated before the first expires, the WDT generates an external timeout signal and optionally initiates an internal interrupt through location '60. After a delay of about 100 ms, the WDT also has the ability to initiate an optional system reset/auto restart cycle.

The various sections of the clock can be used independently or at the same time according to the bit pattern loaded into a common control register. Figure 5-6 shows interrelationships and the controlling PIO instructions. Control register bit assignments are shown in Figure 5-7.

Common Instructions

The following instructions apply to all of the clock sections.

NOTE

The standard device address of the three clock sections is '20. As a result, INA and OTA instructions are always ready and do not skip. If a second SOC is added, all INA and OTA instructions are always ready and do skip.

OCP '1520 Set Interrupt Mask

Enables either the LFC or PIC interrupt, whichever is active.

OCP '1620 Reset Interrupt Mask

OCP '1720 Initialize

Has the same effect as a system reset:

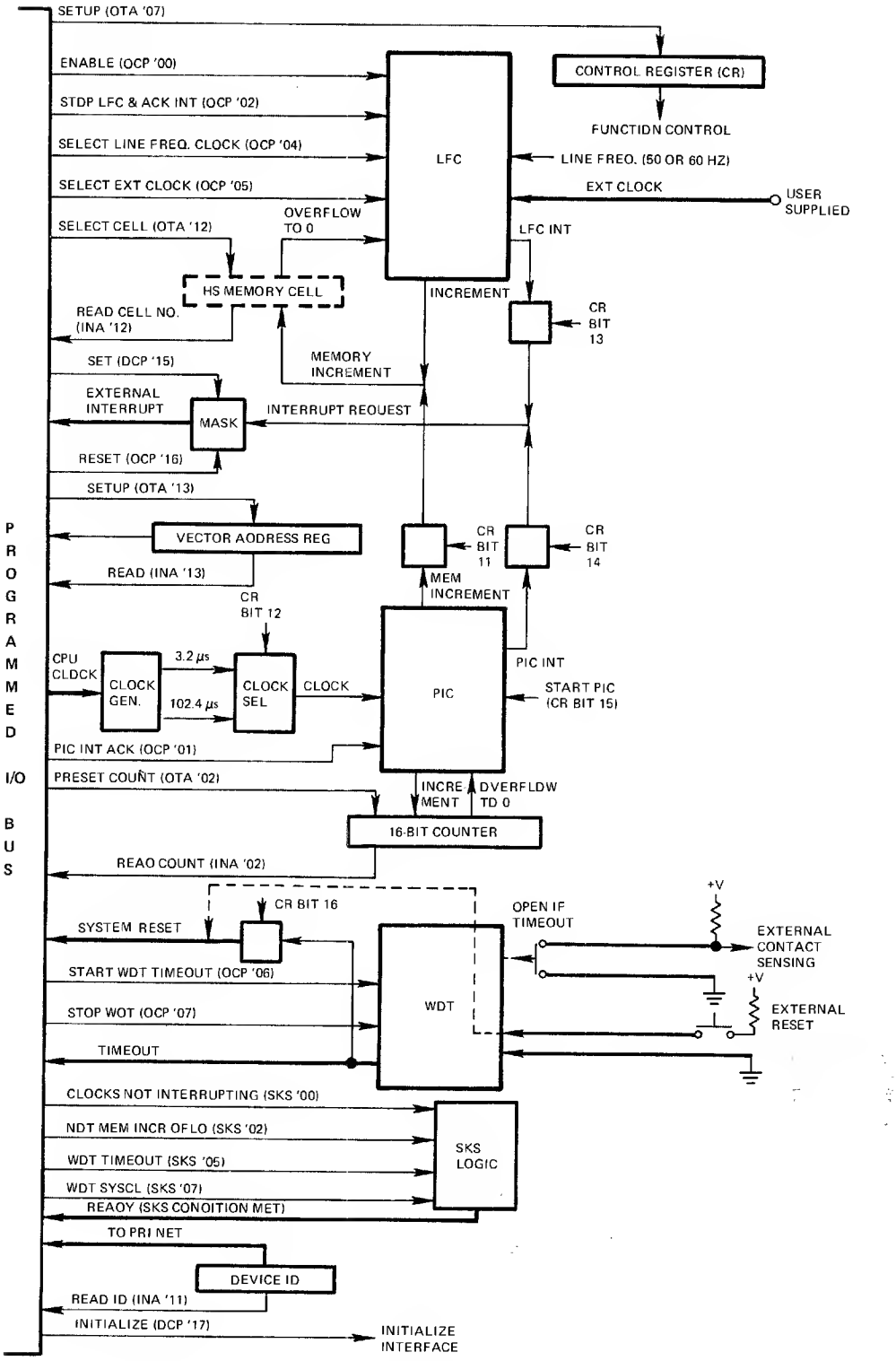


Figure 5-6. LFC, PIC and WDT Block Diagram

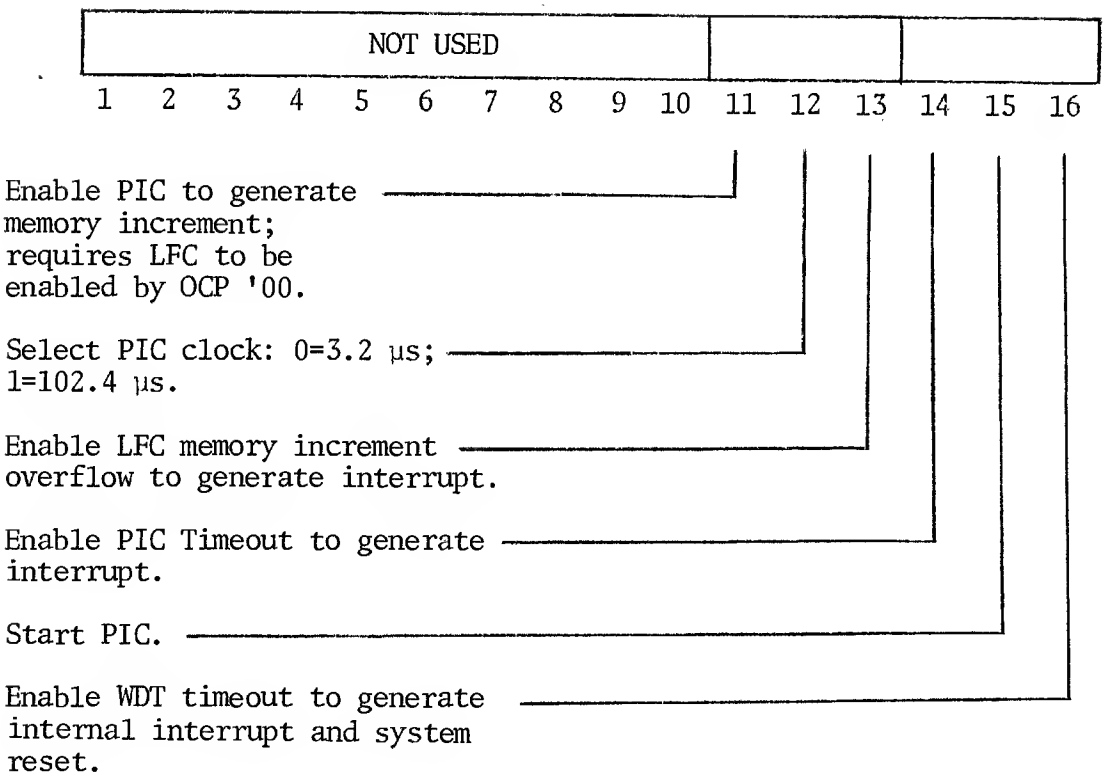


Figure 5-7. LFC, PIC and WDT Control Register Values

LFC stopped

Line frequency selected for LFC memory increment

Memory increment overflow selected to generate interrupts

Interrupt mask cleared

PIC disabled (stopped)

3.2 μs clock selected for PIC

PIC disabled from causing interrupts

WDT timeout disabled from generating system reset

SKS '0200 Skip if LFC or PIC Not Interrupting

INA '1120 Input device ID

The ID of this option is '120.

INA '1320 Input Interrupt Vector

OTA '0720 Load Control Register

See Figure 5-8.

OTA '1320 Load Interrupt Vector

Bits 1-4 must be 0.

Line Frequency Clock

The Line Frequency Clock (LFC) is a simple interval timer that provides a source of interrupts at program-selectable intervals. The LFC determines time intervals by incrementing a program-selected memory location at a selected clock rate and detecting overflow to zero. Incrementing is done by a memory-increment interrupt cycle automatically interleaved with normal program execution. The time interval may be preset by loading the selected location with the 2's complement of the desired number of clock periods. The incrementing timebase is obtained from one of three sources:

Source	Rate
Power Line Frequency	50 or 60 Hz, depending on local frequency
External Clock	User supplied (3 μs minimum period)
PIC Overflow	Program controlled

When the increment location overflows to all zeros, the LFC issues an external interrupt request, if masked on. In standard interrupt mode, the processor responds with an indirect JST through location '63. In vectored mode, the LFC supplies the current vector address as the pointer to the LFC service routine.

The LFC is controlled by instructions which enable and disable memory incrementing, enable and disable the overflow interrupt, and send status information to the CPU.

OCP '0020 Start LFC and Enable Memory Increment

This enables the LFC memory increment function and acknowledges the previous memory increment overflow interrupt.

OCP '0220 Stop LFC and Disable Memory Increment

This disables the LFC memory increment function and acknowledges any previous memory increment overflow interrupt.

OCP '0420 Select Line Frequency for Memory Increment

OCP '0520 Select External Clock for Memory Increment

When both external clock and PIC are selected for memory increment, this instruction enables a diagnostic mode in which any OTA to this controller causes a memory increment.

SKS '0220 Skip if Interrupt Not Memory Increment Overflow

INA '1220 Input Memory Increment Cell Address

OTA '1220 Load Address of Increment Memory Cell

Bits 1-4 must be 0.

Programmable Interval Clock (PIC)

The PIC increments a 16-bit counter at one of two clock rates, 3.2 μs or 102.4 μs. When the register overflows from -1 to 0, the PIC initiates an external interrupt, or increments the LFC memory cell, or both, and reloads the counter with the preset interval. The maximum time interval is 200 ms with the 3.2 μs clock or 6.7 seconds with the 102.4 μs clock. The current value of the PIC register is available to the program. The interrupt vector is the same as that used by the LFC and is differentiated from it by a sense instruction.

OCP '0120	Acknowledge PIC Interrupt
INA '0220	Input PIC Clock Register
OTA '0220	Set PIC Interval Register

The number entered is the 2's complement of the number of counts prior to overflow. This value is stored and preset into the counter again after every overflow.

Watchdog Timer

The watchdog timer guards against a program being caught in endless loops or stalled by an I/O malfunction. When the WDT is operational, it must be triggered by an OCP instruction at least every 50 milliseconds. If the program fails to retrigger the WDT within 50 ms, a timeout occurs and an external timeout signal is generated. If enabled by control register bit 16, an internal interrupt is initiated through location '60 (same as PFI). About 1 millisecond is allowed for saving the machine state or whatever other orderly shutdown operations are required. During this interval, SKS '0720 will skip to indicate that the WDT caused the interrupt. An automatic system clear and auto-restart then occurs, if enabled. Figure 5-8 shows the relative timing of the events that follow a WDT timeout.

The WDT is provided with four external lines. Two of these signal a timeout and the other two are used to initiate a system reset/auto-load.

The WDT should always be stopped when power is applied as system reset does not reset the internal registers.

When the system reset is initiated by the external contact, the WDT continues to generate system resets until the closure is removed. This may result in multiple powerfail interrupts and multiple auto restart/auto loads.

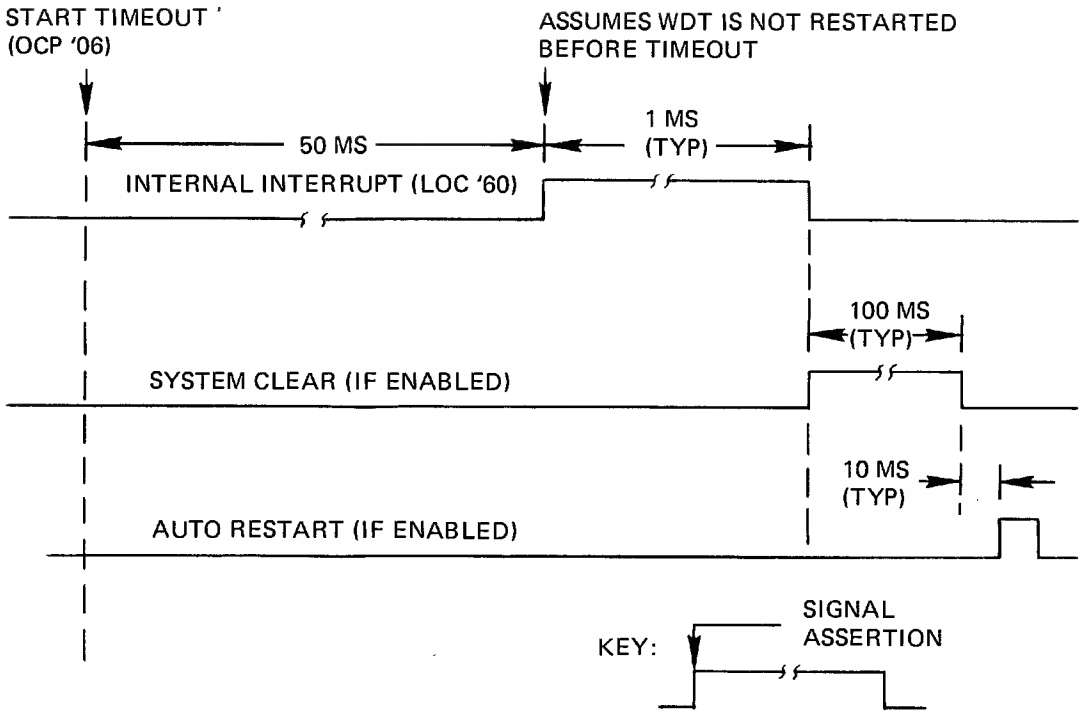


Figure 5-8. Watchdog Timer Time Relationships

OCP '0620 Trigger WDT

Starts the 50 millisecond timeout if the WDT was stopped, or restarts a new 50 millisecond timeout if the WDT was running.

OCP '0720 Stop WDT

SKS '0520 Skip if WDT Timed Out

SKS '0720 Skip if WDT Caused Internal Interrupt (Loc. '60)

SECTION 6

TEST AND MAINTENANCE

This section describes how to use standard Prime diagnostic tests used for factory and on-site checkout of this controller. Tests are supplied in the T&M UFD of master disk Volume 1 or on paper tapes:

Filename in T&M UFD	Tests	Paper Tape	Low	High	Start
TTYT2	Serial Interface using SOC Port No. 1	SLT0783.004	60	11313	1000
BPIOT1	Buffered Parallel I/O Chan. 1 and 2 in Diagnostic Mode	SLT0768.002	60	3732	1000
RTCT2	Real Time Clock functions	SLT0784.003	60	5051	1000

LOADING TEST PROGRAMS

To load tests under DOS, attach to the T&M UFD and RESUME the test. (Files in T&M are binary run files.) In a paper tape system, use APL to load the self-loading tape.

NOTE

Do not attempt to run test programs under DOS/VM.

SERIAL INTERFACE

Standard asynchronous device controller test TTYT2 checks out the serial interface in asynchronous (and optionally synchronous) operating modes. Diagnostic mode is used to test internal controller functions. For best results, a terminal should be connected to Port No. 1 for operational tests in normal mode.

Following is a brief description of the TTYT2 functions and an example of the dialog at a terminal. If errors are encountered the CPU halts; to diagnose the problem, consult the listing and interpret the comments at the halt location.

Test Selection

TTYT2 performs several functional tests of the SOC serial interface both in diagnostic mode and in normal mode using the terminal as an input/output device. The tests are selected by CPU sense switch settings made before the test is started:

SS6	Set to ignore machine check
SS7	Set for ASR 35, reset for 33
SS8	Bypass function test if set
SS9	Bypass page printer test if set
SS10	Bypass keyboard input test if set
SS11	Bypass answerback drum test if set
SS12	Bypass null character test if set
SS13	Bypass punch test if set
SS14	Bypass reader test if set
SS15	Bypass device ID print routine if set

Function Test Routine: Tests the interface to ensure that the instruction subset is operational. After initial tests, a baud rate test is performed. The test data pattern (0-377) for each baud rate is displayed. This is repeated once. The program also checks all normal mode instructions and functions.

Page Printer/Display: Prints up to 70 lines (70 columns/line) of rotating patterns, and then prints a full line for every character printed in the first line of the rotating pattern. Each test may be terminated by depressing any data switch.

Keyboard Input: Waits for a line to be typed at the keyboard, followed by a .CR., and then prints a duplicate of the line plus a character count.

In addition, a full duplex keyboard test is performed in which each character that the operator types in is echoed back one character at a time via software. The output lags the input by one character to demonstrate full duplex operation. A carriage return eliminates the keyboard input.

Answer Back Drum Test: An output code - WRU (205) - is sent to the ASR; the program then counts and prints the number of interrupts received. Acceptable responses are 0 (option disabled) or 20.

Null Character Test: A data string of null characters is output to verify that they do not print.

Punch Test: Punches a data string of X and Z patterns to check out all punch and reader channels. Following this is a stop code character set and an identification character for ASR-33 or 35. An incrementing binary pattern is then punched under interrupt control.

If the device is an ASR-33, the program requests the operator to turn on the punch. At the end of the data patterns, some trailer will be punched along with a message to turn off the punch (for 33 only). This message is not part of the test data.

Reader Test: Tests the tape generated by the punch test. On entry, the program requests the operator to load the test tape and press start. Set the reader controls as follows:

ASR-33	Free stop start switch on stop
ASR-35	Free stop run switch on run, also set mode switch to T.

As in the punch routine, this test is under interrupt control. Data read is placed in a buffer and is checked after the entire block has been input. Error information is presented prior to reading the next data string. Errors detected as part of the stop code test cause a halt as soon as detected.

Device ID Print Routine: Tests all possible device addresses and prints the code for those that respond.

Operating Procedures

1. Make sure the terminal power is on. A Teletype should be in LINE mode.

2. Master clear the CPU and select tests by the sense switch settings previously described.

3. If the SOC device address is other than the standard '04, set the new value in the A Register before starting tests.

4. Press CPU START to begin tests. Respond to the terminal dialog to enter test strings and interpret results. The test asks two questions before starting - TEST SLC? (test synchronous capability) and TEST DMA?. Respond Y to perform test, N if not.

Example

Following is an example of a TTYT2 test run with reader and punch tests suppressed. User input is underlined.

```
TEST SLC ?
N

TEST DMA ?
Y
TESTING DMA

END FUNCTION TEST DEVICE ADDRESS 000004

KEYBOARD INPUT
1QAZXSW23EDCVFR45TGBNHY67UJM,KI.90L./;P0:-
1QAZXSW2CEDCVFR45TGBNHY67UJM,KI090L./;P0:-
CHARACTER COUNT =      42
FULL DPLX KEYBOARD TEST
1QAZ2WXSH
1QAZ2WXSH
CHARACTER COUNT =       9

TEST FOR ANSWER BACK DRUM
CHARACTER COUNT =       0
NULL TEST-NOTHING SHOULD PRINT

DONE
DEVICE 000001 HAS ID 000001
DEVICE 000004 HAS ID 000104
DEVICE 000020 HAS ID 000120
DEVICE 000030 HAS ID 000121
DEVICE 000031 HAS ID 000102


PAGE PRINTER TEST

 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJ

!!!!!!!!!!
INITIAL SSW'S WERE  000014
MAKE NEW SELECTION

END TTYT2 REV 05
```

BPIOC TEST PROGRAM

Standard Prime test program BPIOT1 tests both BPIOC channels on a SOC board in diagnostic mode. It checks operation of the instruction set and simulates input/output transfers but does not check out the interface to external devices. This test should be run with external cabling disconnected.

There are no sense switch settings. Test conditions are set up by a dialog at the system terminal in which the device addresses of both BPIOC's are specified and the user is given the option of testing transfers in DMC mode. (See example.)

Operating Procedure

1. Load BPIOT1
2. Master clear the CPU
3. Press CPU START
4. Respond to the cues at the system terminal; enter the device addresses and specify whether to test DMC functions. (See example.)

Example

(User input is underlined).

```
BPIOT1 REV Ø3

ENTER BPIOC #1 DEVICE ADDRESS  (OCTAL NUMBER THEN CR)
30

ENTER BPIOC #2 DEVICE ADDRESS  (OCTAL NUMBER THEN CR)
31

TEST DMA ? (TYPE Y OR N THEN CR)
Y

DEVICE ØØØØØ1 HAS ID ØØØØØ1
DEVICE ØØØØØ4 HAS ID ØØØ1Ø4
DEVICE ØØØØ2Ø HAS ID ØØØ12Ø
DEVICE ØØØØ3Ø HAS ID ØØØ1Ø1
DEVICE ØØØØ31 HAS ID ØØØ1Ø2

END BPIOT1 REV Ø3
```

REAL TIME CLOCK TEST

Prime diagnostic test RTCT2 checks out the LFC portion of the real time clock interface and optionally tests the PIC and WDT. Following is a brief description of its functions and an example of the dialog at the terminal. If errors are encountered the CPU halts; to diagnose the problem, consult the listing and interpret the comments at the halt location. Error halts ER27 and ER28 indicate out of tolerance line frequency.

RTCT2 tests the RTC logic for proper initialization after a master clear, and then progresses through a series of tests to verify each of the commands, SKS's, memory increment, and interrupt in compatible and vectored modes. Each test is designed to test one function at a time for ease of isolation.

After the controller test has been completed, the program determines the line frequency and displays an incrementing count of one count per second (SSW 16 reset) or one count every 15 seconds (SSW 16 set). During this display, each RTC cycle is checked to verify that only one increment is received per line cycle. The program accepts line frequencies of 47-54 Hz and 57-63 Hz.

Sense Switches

SSW 1-5, 7-15	Not Used.
SSW 6	Set to run out of machine check mode.
SSW 16	Set to count each 15 seconds, reset to count each second.

Operating Procedure

1. Master clear the CPU.
2. Set sense switches as described above.
3. Press CPU START.
4. Respond to the queries at the system terminal:

Device Address	Enter the device address in octal. The standard address is '20.
PIC	Type Y to test Programmable Internal Clock, N if not.
WDT	Type Y to test Watchdog Timer (N if not).

Example

(User input is underlined)

```
RTCT2 - TEST AND VERIF. - S0C -10-01-74

TYPE IN OCTAL DEVICE ADDRESS
20
DEVICE ADDRESS IS 000020

TEST PIC ? (TYPE Y OR N THEN CR)
Y

TEST WDT ? (TYPE Y OR N THEN CR)
Y

DEVICE 000001 HAS ID 000001
DEVICE 000004 HAS ID 000104
DEVICE 000020 HAS ID 000120
DEVICE 000030 HAS ID 000101
DEVICE 000031 HAS ID 000102

END RTCT2 REV 03
```

APPENDIX A

BPIOC OPTION JUMPERS

Many functions of the BPIOC channels on the SOC board are defined by jumper connections at DIP sites. Tables A-1 through A-4 show the available options. Standard factory wiring is identified by asterisks.

DIP sites for jumpers are identified by column (numerical) and row (alphabetical) and the pins are those of the DIP site. For example, 21K-2 refers to pin 2 of the DIP at column 21, row K.

Certain one-shot delays can also be modified by capacitor changes. These can be located on the logic diagrams as follows:

Mnemonic			
BPIOC 1	BPIOC 2	Delay	Nominal Value
B1C1 B1RC1	B2C1 B2RC1	Delay before BPIOC takes input data	3 µs
B1C3 B1RC3	B2C3 B3RC3	Delay from the time output data is stable to D1MVR/R, D2MVF/R	3 µs
B1C4 B1RC4	B2C4 B2RC4	D1MVF/R, D2MVF/R pulse width	User determined if pulse option is used

Capacitor Locations

Board Type	Channel	Capacitor Location
Wire Wrap	BPIOC1	6L
	BPIOC2	18L
Etch	BPIOC1	1K
	BPIOC2	17H

Table A-1. BPIOC No. 1 Jumpers, Etched Board

Jumper			Function
From	To		
9K-15	9K-2		Initialize in output mode
9K-3	9K-14		
9K-15	9K-1	*	Initialize in input mode
9K-3	9K-13	*	
9K-9	9K-5	*	16-bit input
	9K-7		8-bit input transfers
IN-2	IN-14		D1SKS + true
	IN-15	*	D1SKS - true
IM-10	IM-6		D1OTA + true
	IM-7	*	D1OTA - true
IN-13	IN-4		D1RDY + true
	IN-3	*	D1RDY - true
IM-2	IM-14		D1MVF + true
	IM-15	*	D1MVF - true
IM-4	IM-13		D1MVR + true
	IM-12	*	D1MVR - true
			D1STRB edge to generate D1MVF if ready:
IN-5	IN-11	*	⌐ input, ¬ output
	IN-12		¬ input, ⌐ output

* STANDARD FACTORY WIRING

Table A-1. (Cont)

Jumper			Function
From	To		
IN-7	IN-10	*	Edge of DISTRB to take data (input) or acknowledge data taken (output): ⌐¬ input, ¬⌐ output
	IN-9		¬⌐ input, ⌐¬ output
5J-12	5J-4	*	DIMVF, DIMVR are levels for handshake
	5J-5		DIMVF, DIMVR are pulses
5J-6	5J-10		DIMVF, DIMVR are mutually exclusive
	5J-11	*	Control register bit 15 determines whether DIMVR is generated
5J-2	5J-15	*	Use DISTRB to acknowledge data being taken by device
	5J-14		Use for byte packing in non-handshake interface (see logic diagrams)

* STANDARD FACTORY WIRING

Table A-2. BPIOC No. 1 Jumpers, Wire Wrap Board

Jumper			Function
From	To		
12M-15	12M-1		Initialize in output mode
12M-3	12M-14		
12M-15	12M-2	*	Initialize in input mode
12M-3	12M-13	*	
12M-9	12M-8	*	16-bit input
	12M-7		8-bit input transfers
12M-12	12M-4		D1SKS + true
	12M-5	*	D1SKS - true
12M-6	12M-10		D1OTA + true
	12M-11	*	D1OTA - true
10M-3	10M-13		D1RDY + true
	10M-14	*	D1RDY - true
10M-12	10M-4		D1MVF + true
	10M-5	*	D1MVF - true
10M-6	10M-10		D1MVR + true
	10M-11	*	D1MVR - true
10M-15			D1STRB edge to generate D1MVF if ready:
	10M-1	*	⌐ input, ¬ output
	10M-2		¬ input, ⌐ output

* STANDARD FACTORY WIRING

Table A-2. (Cont)

Jumper			Function
From	To		
10L-15	10L-1	*	Edge of DISTRB to take data (input) or acknowledge data taken (output): ⌐input, ⌐output
	10L-2		⌐input, ⌐output
10L-12	10L-4	*	DIMVF, DIMVR are levels for handshake
	10L-5		DIMVF, DIMVR are pulses
10L-6	10L-10		DIMVF, DIMVR are mutually exclusive
	10L-11	*	Control register bit 15 determines whether DIMVR is generated
10L-3	10L-13	*	Use DISTRB to acknowledge data being taken by device
	10L-14		Use for byte packing in non-handshake interface (see logic diagrams)

* STANDARD FACTORY WIRING

Table A-3. BPIOC No. 2 Jumpers, Etch Board

Jumper			Function
From	To		
21K-15	21K-2		Initialize in output mode
21K-14	21K-4		
21K-15	21K-1	*	Initialize in input mode
21K-14	21K-3	*	
21K-9	21K-8	*	16-bit input
	21K-7		8-bit input transfers
15K-12	15K-4		D2SKS + true
	15K-5	*	D2SKS - true
17K-6	17K-11		D2OTA + true
	17K-10	*	D2OTA - true
15K-3	15K-14		D2RDY + true
	15K-13	*	D2RDY - true
17K-12	17K-4		D2MVF + true
	17K-5	*	D2MVF - true
17K-2	17K-15		D2MVR + true
	17K-14	*	D2MVR - true
15K-15			D2STRB edge to generate D2MVF if ready
	15K-1	*	⌐ input, ¬ output
	15K-2		¬ input, ⌐ output

* STANDARD FACTORY WIRING

Table A-3. (Cont)

Jumper			Function
From	To		
15K-11	15K-7	*	Edge of D2STRB to take data (input) or acknowledge data taken (output): ⌐ input, ⌐ output
	15K-6		⌐ input, ⌐ output
21K-11	21K-6	*	D2MVF, D2MVR are levels for handshake
	21K-5		D2MVF, D2MVR are pulses
23J-5	23J-11		D2MVF, D2MVR are mutually exclusive
	23J-12	*	Control register bit 15 determines whether D2MVR is generated
23J-10	23J-6	*	Use D2STRB to acknowledge data being taken by device
	23J-7		Use for byte packing in non-handshake interface (see logic diagrams)

* STANDARD FACTORY WIRING

Table A-4. BPIOC No. 2 Jumpers, Wire Wrap Board

Jumper		Function
From	To	
12L-15	12L-1	Initialize in output mode
12L-3	12L-14	
12L-15	12L-2	* Initialize in input mode
12L-3	12L-13	*
12L-9	12L-8	* 16-bit input
	12L-7	8-bit input transfers
12L-12	12L-4	D2SKS + true
	12L-5	* D2SKS - true
12L-6	12L-10	D2OTA + true
	12L-11	* D2OTA - true
14M-3	14M-13	D2RDY + true
	14M-14	* D2RDY - true
14M-12	14M-4	D2MVF + true
	14M-5	* D2MVF - true
14M-6	14M-10	D2MVR + true
	14M-11	* D2MVR - true
14M-15	14M-1	D2STRB edge to generate D2MVF if ready:
		* ⌜ input, ⌞ output
	14M-2	⌞ input, ⌜ output

* STANDARD FACTORY WIRING

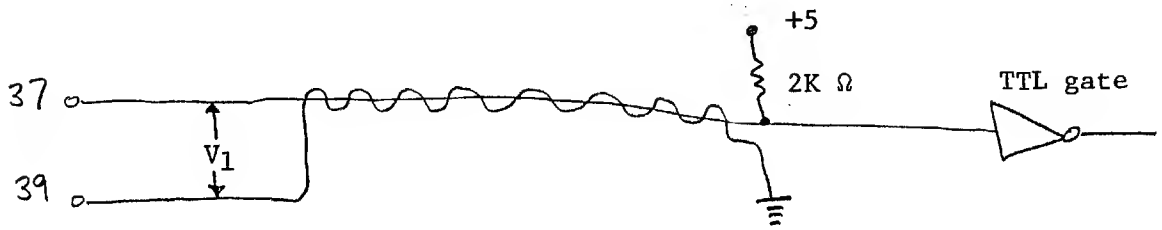
Table A-4. (Cont)

Jumper			Function
From	To		
			Edge of D2STRB to take data (input) or acknowledge data taken (output):
14L-15	14L-1	*	⌐_ input, _⌐ output
	14L-2		_⌐ input, ⌐_ output
14L-12	14L-4	*	D2MVF, D2MVR are levels for handshake
	14L-5		D2MVF, D2MVR are pulses
14L-6	14L-10		D2MVF, D2MVR are mutually exclusive
	14L-11	*	Control register bit 15 determines whether D2MVR is generated
14L-3	14L-13	*	Use D2STRB to acknowledge data being taken by device
	14L-14		Use for byte packing in non-handshake interface (see logic diagrams)

* STANDARD FACTORY WIRING

SOC WDT

The following circuit is recommended when the WDT output (opto-isolator) is used to drive a TTL input



The use of a 2K Ω pull-up resistor and one TTL gate load (1.6 ma) will guarantee that V_1 is < .4V.

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PRIME

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